

IN74AC164

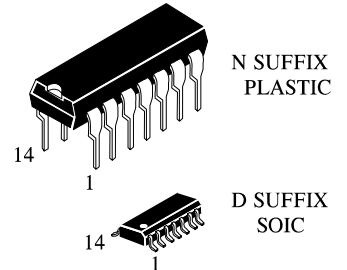
8-Bit Serial-Input/Parallel-Output Shift register

High-Speed Silicon-Gate CMOS

The IN74AC164 is identical in pinout to the LS/ALS164, HC/HCT164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

The IN74AC164 is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

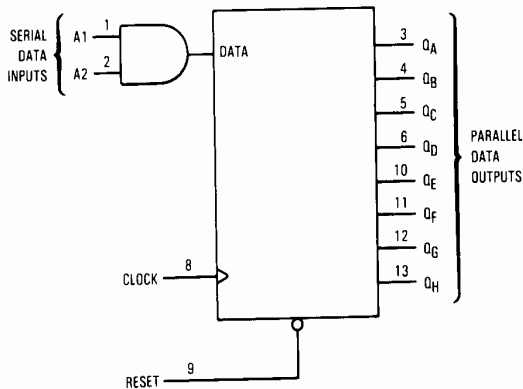


ORDERING INFORMATION

IN74AC164N Plastic
IN74AC164D SOIC

$T_A = -40^\circ$ to 85° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1	14	V_{CC}
A2	2	13	QH
QA	3	12	QG
QB	4	11	QF
QC	5	10	QE
QD	6	9	RESET
GND	7	8	CLOCK

FUNCTION TABLE

Inputs				Outputs		
Reset	Clock	A1	A2	Q_A	Q_B	...
L	X	X	X	L	L	... L
H		X	X	no change		
H		H	D	D	Q_{An}	...
H		D	H	D	Q_{An}	...

D = data input
X = don't care
 $Q_{An} - Q_{Gn}$ = data shifted from the previous stage on a rising edge at the clock input.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	$^{\circ}C$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

SOIC Package: : - 7 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V	
T_J	Junction Temperature (PDIP)		140	$^{\circ}C$	
T_A	Operating Temperature, All Package Types	-40	+85	$^{\circ}C$	
I_{OH}	Output Current - High		-24	mA	
I_{OL}	Output Current - Low		24	mA	
t_r, t_f	Input Rise and Fall Time * (except Schmitt Inputs)	$V_{CC} = 3.0$ V $V_{CC} = 4.5$ V $V_{CC} = 5.5$ V	0 0 0	150 40 25	ns/V

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V	3.0	2.1	2.1	V
			4.5	3.15	3.15	
			5.5	3.85	3.85	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V	3.0	0.9	0.9	V
			4.5	1.35	1.35	
			5.5	1.65	1.65	
V _{OH}	Minimum High-Level Output Voltage	I _{OUT} ≤ -50 μA	3.0	2.9	2.9	V
			4.5	4.4	4.4	
			5.5	5.4	5.4	
		*V _{IN} =V _{IH} or V _{IL} I _{OH} =-12 mA	3.0	2.56	2.46	
		I _{OH} =-24 mA I _{OH} =-24 mA	4.5	3.86	3.76	
5.5	4.86	4.76				
V _{OL}	Maximum Low-Level Output Voltage	I _{OUT} ≤ 50 μA	3.0	0.1	0.1	V
			4.5	0.1	0.1	
			5.5	0.1	0.1	
		*V _{IN} =V _{IH} or V _{IL} I _{OL} =12 mA	3.0	0.36	0.44	
		I _{OL} =24 mA I _{OL} =24 mA	4.5	0.36	0.44	
5.5	0.36	0.44				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	μA
I _{OLD}	+Minimum Dynamic Output Current	V _{OLD} =1.65 V Max	5.5		75	mA
I _{OHD}	+Minimum Dynamic Output Current	V _{OHD} =3.85 V Min	5.5		-75	mA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND	5.5	4.0	40	μA

* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

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AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (Figure 1)	3.3 5.0	125 150		100 125		MHz
t_{PLH}	Propagation Delay, Clock to Q (Figure 1)	3.3 5.0	4.0 2.5	13.5 10.0	3.5 2.0	16.0 10.5	ns
t_{PHL}	Propagation Delay, Clock to Q (Figure 1)	3.3 5.0	3.0 2.0	14.0 10.0	3.0 1.5	14.5 10.5	ns
t_{PHL}	Propagation Delay, Reset to Q (Figure 2)	3.3 5.0	3.0 2.0	12.0 9.5	3.0 2.0	13.5 10.5	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF

C_{PD}	Power Dissipation Capacitance	Typical @25°C, $V_{CC}=5.0\text{ V}$		pF
		35		

*Voltage Range 3.3 V is 3.3 V \pm 0.3 V

Voltage Range 5.0 V is 5.0 V \pm 0.5 V

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limits		Unit	
			25 °C			-40°C to 85°C
			Min	Max		Min
t_{su}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	3.3 5.0	6.5 4.5		7.5 5.0	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	3.3 5.0	0 0.5		0 0.5	ns
t_w	Minimum Pulse Width, Clock or Reset (Figures 1,2)	3.3 5.0	4.0 3.5		4.5 3.5	ns
t_{rec}	Minimum Recovery Time, Reset to Clock (Figure 2)	3.3 5.0	0 0		0 0	ns

*Voltage Range 3.3 V is 3.3 V \pm 0.3 V

Voltage Range 5.0 V is 5.0 V \pm 0.5 V

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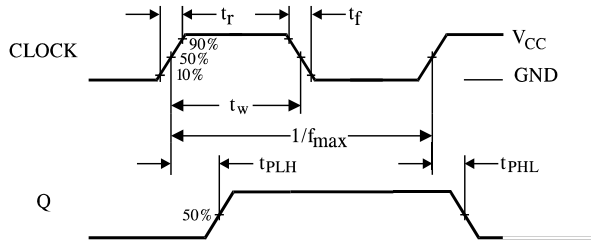


Figure 1. Switching Waveforms

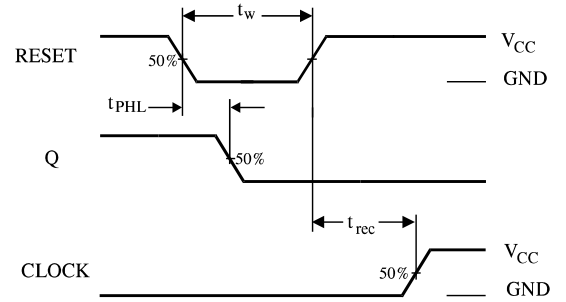


Figure 2. Switching Waveforms

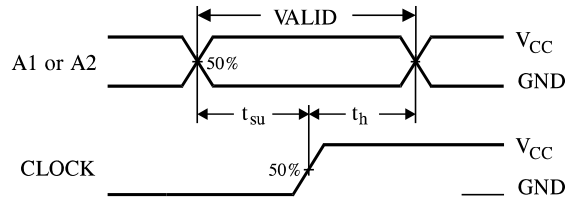
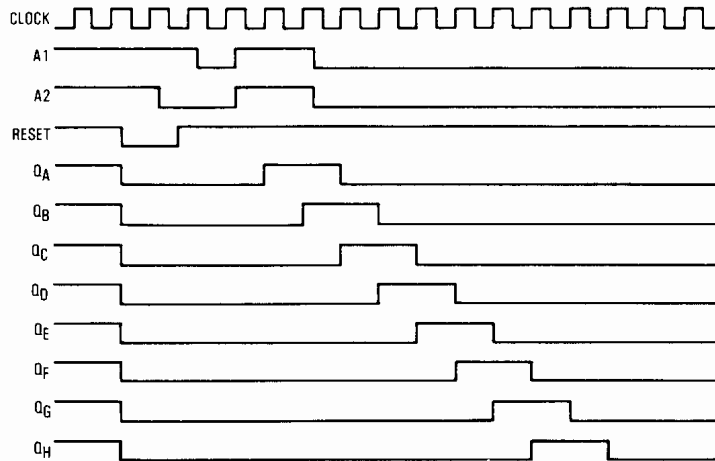
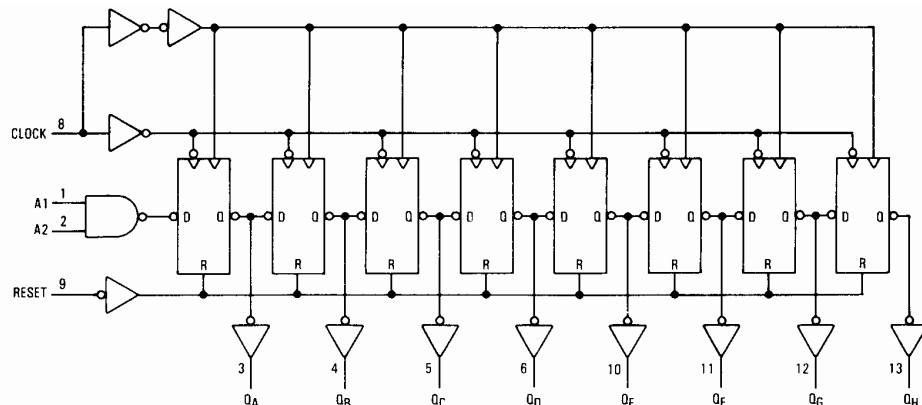


Figure 3. Switching Waveforms
TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



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