

**IN74AC161**

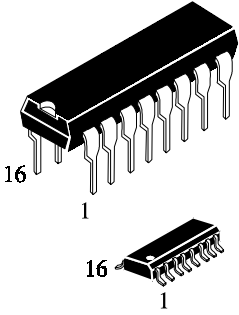
**Pre-settable Counter**  
**High-Speed Silicon-Gate CMOS**

The IN74AC161 is identical in pinout to the LS/ALS161, HC/HCT161. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

The IN74AC161 is programmable 4-bit synchronous modulo-16 counter that feature parallel Load, asynchronous Reset, a Carry Output for cascading and count-enable controls.

The IN74AC161 is binary counter with asynchronous Reset.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A; 0.1  $\mu$ A @ 25° C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

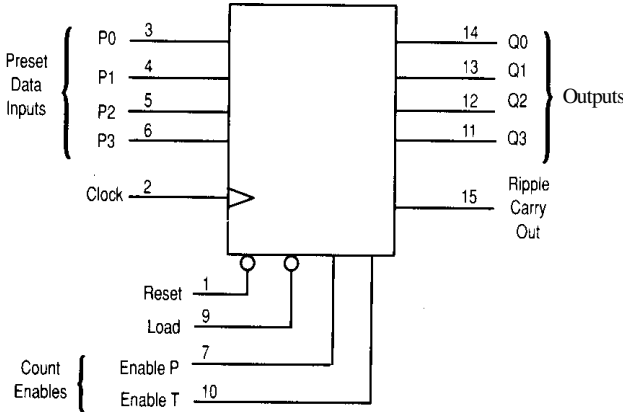


**N SUFFIX PLASTIC**

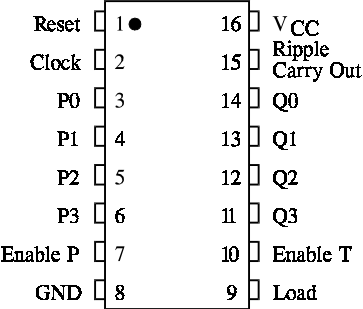
**D SUFFIX SOIC**

**ORDERING INFORMATION**  
IN74AC161N Plastic  
IN74AC161D SOIC  
 $T_A = -40^\circ$  to  $85^\circ$  C for all packages

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**



PIN 16 =  $V_{CC}$   
PIN 8 = GND

**FUNCTION TABLE**

Inputs					Outputs				Function
Reset	Load	Enable P	Enable T	Clock	Q0	Q1	Q2	Q3	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X		P0	P1	P2	P3	Preset Data
H	H	X	L		No change				No count
H	H	L	X		No change				No count
H	H	H	H		Count up				Count
H	X	X	X		No change				No count

X=don't care  
P0,P1,P2,P3 = logic level of Data inputs  
Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Sink/Source Current, per Pin	±50	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>J</sub>	Junction Temperature (PDIP)		140	°C	
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C	
I <sub>OH</sub>	Output Current - High		-24	mA	
I <sub>OL</sub>	Output Current - Low		24	mA	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time * (except Schmitt Inputs)	V <sub>CC</sub> =3.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =5.5 V	0 0 0	150 40 25	ns/V

\* V<sub>IN</sub> from 30% to 70% V<sub>CC</sub>

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V	3.0	2.1	2.1	V
			4.5	3.15	3.15	
			5.5	3.85	3.85	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> = V <sub>CC</sub> -0.1 V or 0.1 V	3.0	0.9	0.9	V
			4.5	1.35	1.35	
			5.5	1.65	1.65	
V <sub>OH</sub>	Minimum High-Level Output Voltage	I <sub>OUT</sub> ≤ -50 μA	3.0	2.9	2.9	V
			4.5	4.4	4.4	
			5.5	5.4	5.4	
		*V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> =-12 mA	3.0	2.56	2.46	
		I <sub>OH</sub> =-24 mA I <sub>OH</sub> =-24 mA	4.5	3.86	3.76	
5.5	4.86	4.76				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	I <sub>OUT</sub> ≤ 50 μA	3.0	0.1	0.1	V
			4.5	0.1	0.1	
			5.5	0.1	0.1	
		*V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> =12 mA	3.0	0.36	0.44	
		I <sub>OL</sub> =24 mA I <sub>OL</sub> =24 mA	4.5	0.36	0.44	
5.5	0.36	0.44				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	±0.1	±1.0	μA
I <sub>OLD</sub>	+Minimum Dynamic Output Current	V <sub>OLD</sub> =1.65 V Max	5.5		75	mA
I <sub>OHD</sub>	+Minimum Dynamic Output Current	V <sub>OHD</sub> =3.85 V Min	5.5		-75	mA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND	5.5	8.0	8.0	μA

\* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ , Input  $t_r=t_f=3.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}^*$ V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency (Figure 1)	3.3 5.0	70 110		60 95		MHz
$t_{PLH}$	Propagation Delay, Clock to Q (Figure 1)	3.3 5.0	2.0 1.5	12.0 9.0	1.5 1.0	13.5 9.5	ns
$t_{PHL}$	Propagation Delay, Clock to Q (Figure 1)	3.3 5.0	1.5 1.5	12.0 9.5	1.5 1.5	13.0 10.0	ns
$t_{PLH}$	Propagation Delay, Clock to Ripple Carry Out (Figure 1)	3.3 5.0	3.0 2.0	15.0 10.5	2.5 1.5	16.5 11.5	ns
$t_{PHL}$	Propagation Delay, Clock to Ripple Carry Out (Figure 1)	3.3 5.0	3.5 2.0	14.0 11.0	2.5 2.0	15.5 11.5	ns
$t_{PLH}$	Propagation Delay, Enable T to Ripple Carry Out (Figure 3)	3.3 5.0	2.0 1.5	9.5 6.5	1.5 1.0	11.0 7.5	ns
$t_{PHL}$	Propagation Delay, Enable T to Ripple Carry Out (Figure 3)	3.3 5.0	2.5 2.0	11.0 8.5	2.0 1.5	12.5 9.5	ns
$t_{PHL}$	Propagation Delay, Reset to Q (Figure 2)	3.3 5.0	2.0 1.5	12.0 9.5	1.5 1.5	13.5 10.0	ns
$t_{PHL}$	Propagation Delay, Reset to Ripple Carry Out (Figure 2)	3.3 5.0	3.5 2.5	15.0 13.0	3.0 2.5	17.5 13.5	ns
$C_{IN}$	Maximum Input Capacitance	5.0	4.5		4.5		pF

$C_{PD}$	Power Dissipation Capacitance	Typical @25°C, $V_{CC}=5.0\text{ V}$		pF
		45		

\*Voltage Range 3.3 V is 3.3 V  $\pm$ 0.3 V

Voltage Range 5.0 V is 5.0 V  $\pm$ 0.5 V

**TIMING REQUIREMENTS** ( $C_L=50\text{pF}$ , Input  $t_r=t_f=3.0\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> * V	Guaranteed Limit		Unit
			+25° C	-40° C to +85° C	
$t_{su}$	Minimum Setup Time, Preset Data Inputs to Clock (Figure 4)	3.3 5.0	13.5 8.5	16.0 10.5	ns
$t_h$	Minimum Hold Time, Clock to Preset Data Inputs (Figure 4)	3.3 5.0	-1.0 0	-0.5 0	ns
$t_{su}$	Minimum Setup Time, Load to Clock (Figure 4)	3.3 5.0	11.5 7.5	14.0 8.5	ns
$t_h$	Minimum Hold Time, Clock to Load (Figure 4)	3.3 5.0	0 0.5	0 1.0	ns
$t_{su}$	Minimum Setup Time, Enable T or Enable P to Clock (Figure 5)	3.3 5.0	6.0 4.5	7.0 5.0	ns
$t_h$	Minimum Hold Time, Clock to Enable T or Enable P (Figure 5)	3.3 5.0	0 0	0 0.5	ns
$t_w$	Minimum Pulse Width, Clock (Load) (Figure 1)	3.3 5.0	3.5 2.5	4.0 3.0	ns
$t_w$	Minimum Pulse Width, Clock (Count)(Figure 1)	3.3 5.0	4.0 3.0	4.5 3.5	ns
$t_w$	Minimum Pulse Width, Reset (Figure 2)	3.3 5.0	5.5 4.5	7.5 6.0	ns
$t_{rec}$	Minimum Recovery Time, Reset to Clock (Figure 2)	3.3 5.0	-0.5 0	0 0.5	ns

\*Voltage Range 3.3 V is 3.3 V  $\pm$ 0.3 VVoltage Range 5.0 V is 5.0 V  $\pm$ 0.5 V

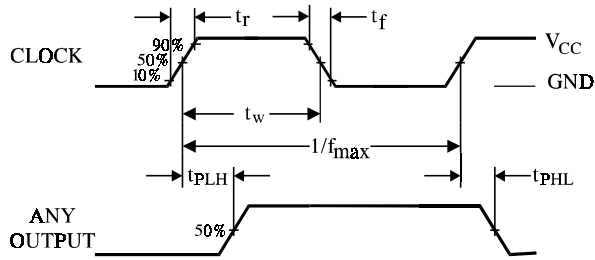


Figure 1. Switching Waveform

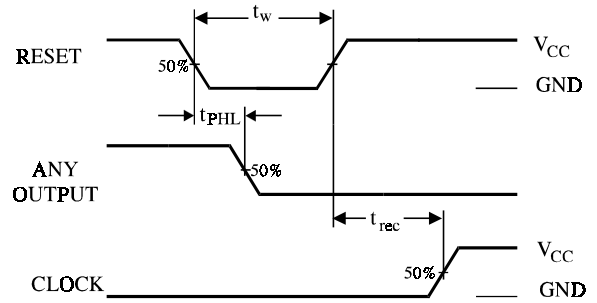


Figure 2. Switching Waveform

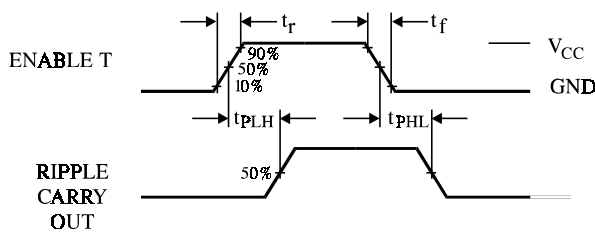


Figure 3. Switching Waveform

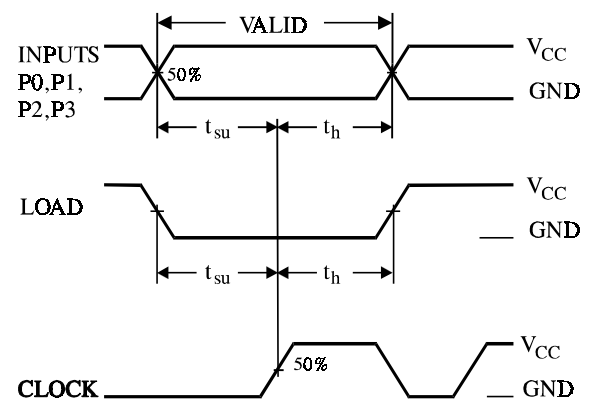


Figure 4. Switching Waveform

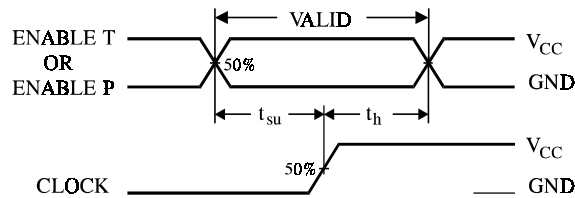
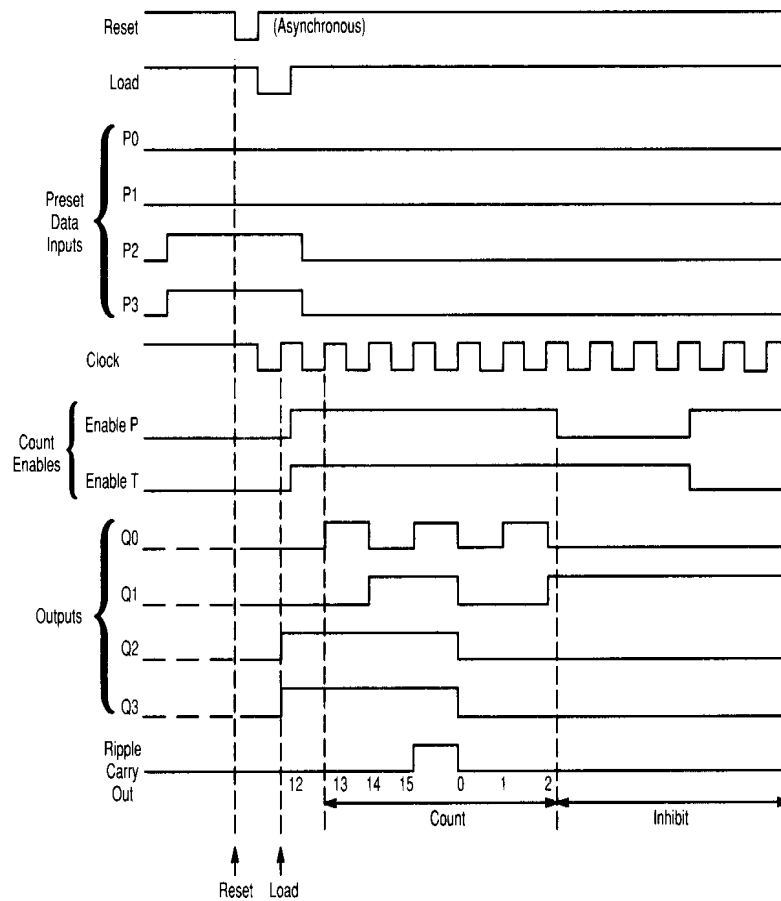


Figure 5. Switching Waveform

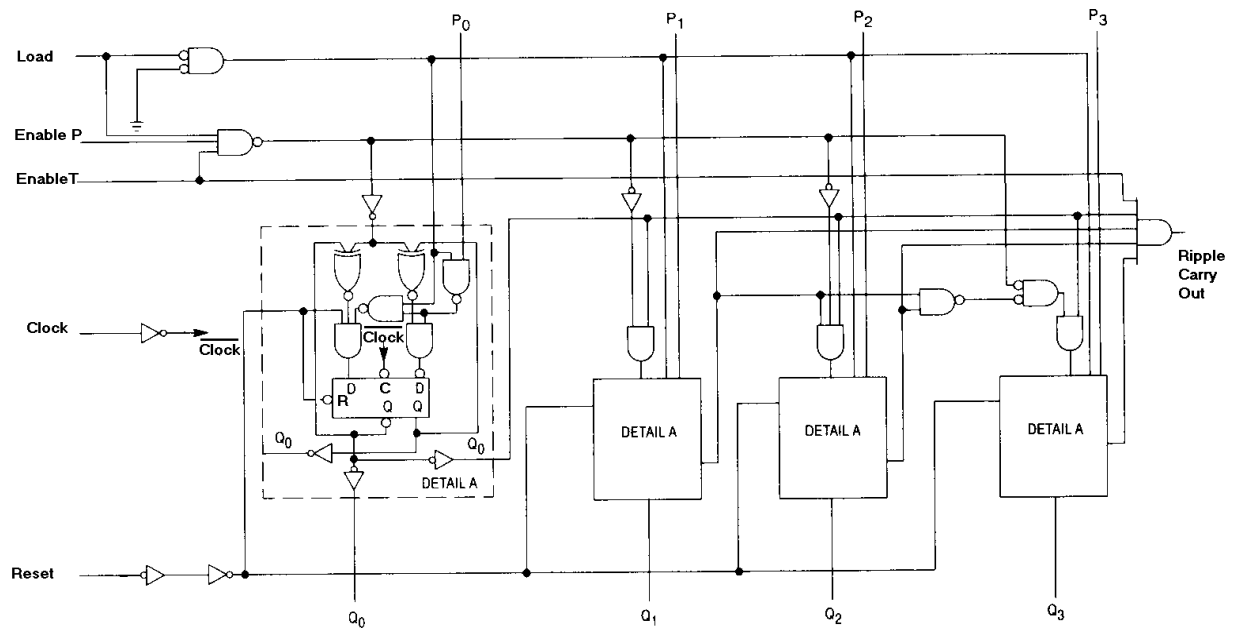


Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

**Figure 8. Timing Diagram**

EXPANDED LOGIC DIAGRAM





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