SONY

CXA1855Q/S

I²C Bus-Compatible Audio/Video Switch

For the availability of this product, please contact the sales office.

Description

The CXA1845Q/S is a 5-input, 3-output audio/video switch featuring I²C bus compatibility for TVs.

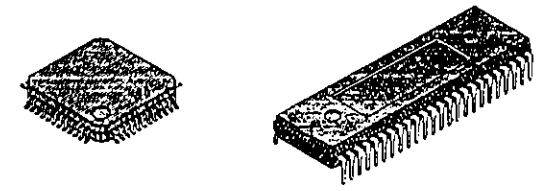
Features

- Serial control with I²C bus
- 5 inputs, 3 outputs
- 3 outputs can each be independently selected
- Separate control of video and audio switches
- 6dB gain amplifiers for video system
- Wideband video amplifier (20MHz, –3dB)
- Y/C mixer circuit
- Slave address can be changed (90H/92H)
- Audio muting from external pin
- High impedance maintained by I²C bus line (SDA, SCL) even when power is OFF
- Wide audio dynamic range (3Vrms typ.)

Applications

Audio/video switch featuring I²C bus compatibility for TVs

CXA1855Q	CXA1855S
48 pin QFP (Plastic)	48 pin SDIP (Plastic)



Absolute Maximum Ratings

• Supply voltage	Vcc	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	PD	750 (QFP)	mW
		1800 (SDIP)	mW

Operating Conditions

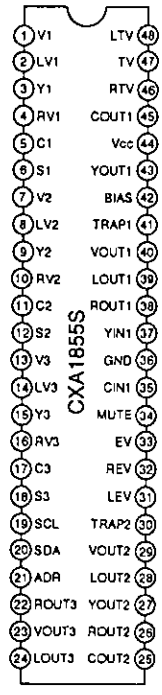
Supply voltage	Vcc	9±0.5	V

Structure

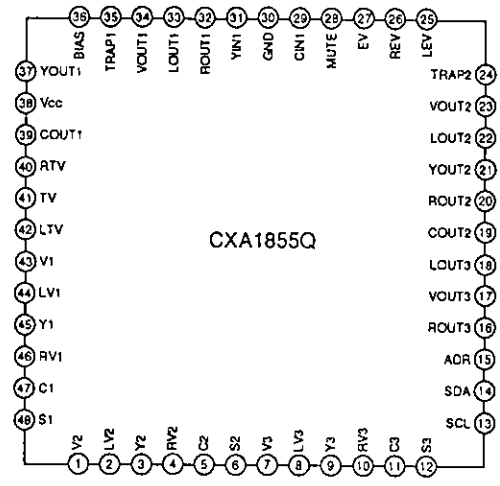
Bipolar silicon monolithic IC

Pin Configuration (Top View)

SDIP 48pin



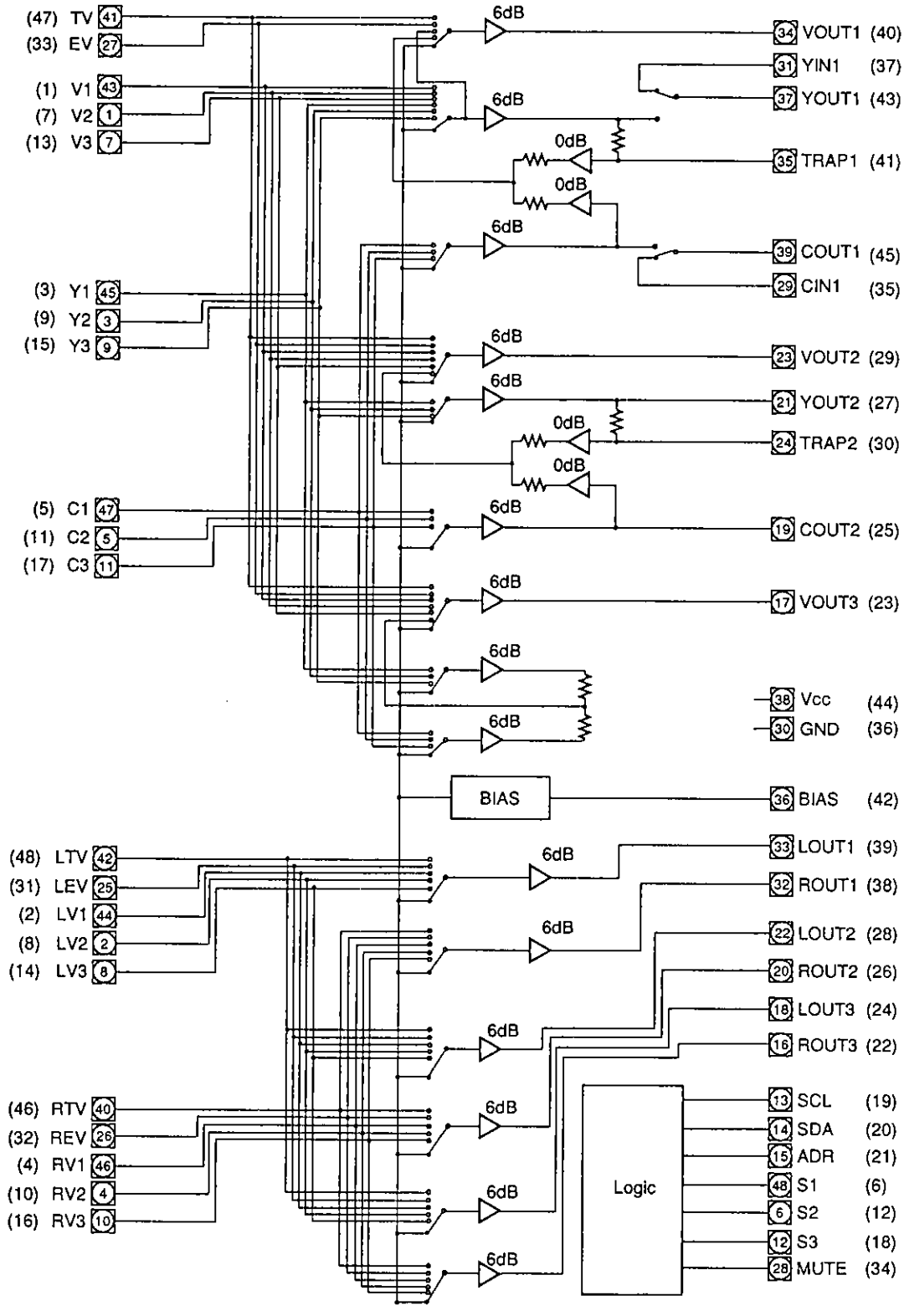
QFP 48pin



E93416B58—ST

Block Diagram

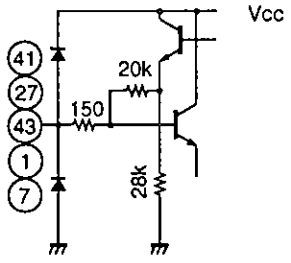
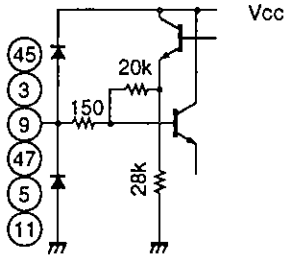
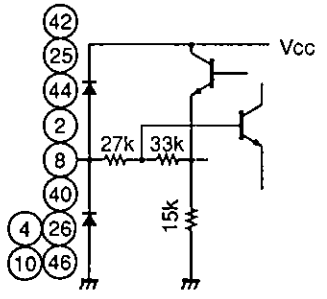
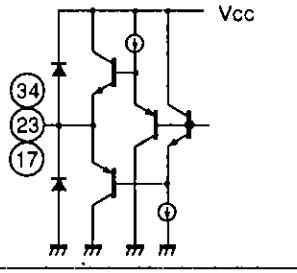
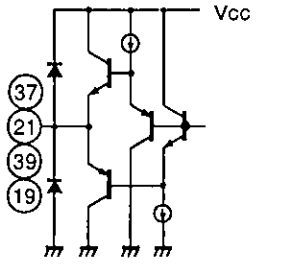
* Parenthesized numbers indicate Pin No. of CXA1855S.

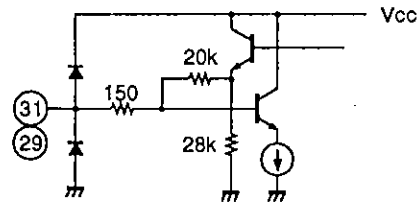
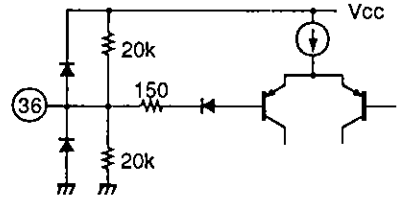
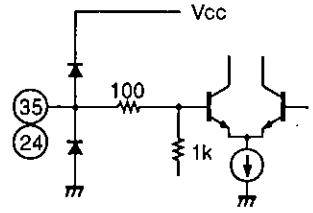
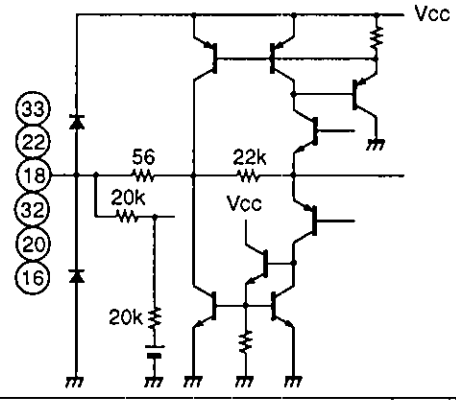
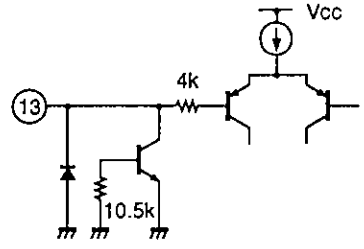


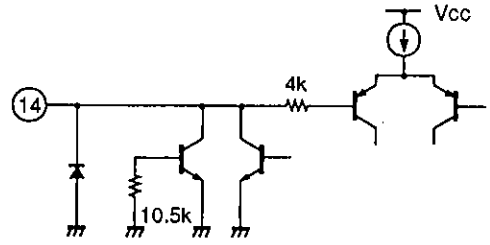
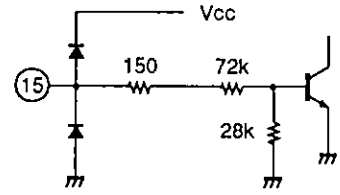
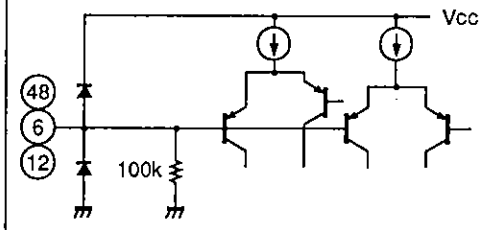
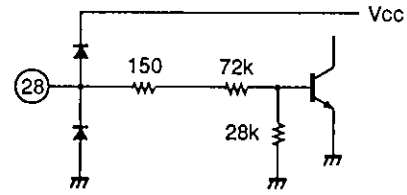
Note) A total gain of 0dB is achieved by connecting a 6kΩ resistor to the each audio input.

Pin Description

Parenthesized numbers indicate Pin No. of CXA1855S

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
41 (47) 27 (33) 43 (1) 1 (7) 7 (13)	TV EV V1 V2 V3	4.5V		Video signal inputs. Input composite video signals.
45 (3) 3 (9) 9 (15) 47 (5) 5 (11) 11 (17)	Y1 Y2 Y3 C1 C2 C3	4.5V		Y/C separation signal inputs Y1 to Y3 pins: Luminance signals input C1 to C3 pins: Chrominance signals input
42 (48) 25 (31) 44 (2) 2 (8) 8 (14) 40 (46) 26 (32) 46 (4) 4 (10) 10 (16)	LTV LEV LV1 LV2 LV3 RTV REV RV1 RV2 RV3	4.6V		Audio signal inputs.
34 (40) 23 (29) 17 (23)	VOUT1 VOUT2 VOUT3	4.5V		Video signal outputs. Output composite video signals.
37 (43) 21 (27) 39 (45) 19 (25)	YOUT1 YOUT2 COUT1 COUT2	4.5V		Y/C signal outputs. YOUT1, YOUT2 pins: Luminance signal output COUT1, COUT2 pins: Chrominance signal output

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31 (37) 29 (35)	YIN1 CIN1	4.5V		Input the Y/C separated signal of VOUT1 output.
36 (42)	BIAS	4.5V		Internal reference bias (Vcc/2). A capacitor is connected between this pin and GND.
35 (41) 24 (30)	TRAP1 TRAP2	4.5V		Connect the subcarrier trap circuits.
33 (39) 22 (28) 18 (24) 32 (38) 20 (26) 16 (22)	LOUT1 LOUT2 LOUT3 ROUT1 ROUT2 ROUT3	4.6V		Audio signal outputs. ZOUT=50Ω (Within DC ±2mA)
13 (19)	SCL	—		I²C bus signal input. VIL=1.5V (max.) VIH=3.0V (min.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14 (20)	SDA	—		I²C bus signal input/output. VIL= 1.5V (max.) VIH= 3.0V (min.) VOL=0.4V (max.)
15 (21)	ADR	—		Selects the slave address for the I²C bus. 90H at 1.5V or less 92H at 2.5V or more 90H when open
48 (6) 6 (12) 12 (18)	S1 S2 S3	—		Video/S signal selection. S signal output at 0.8V or less Video signal output at 1.4V or more S signal output when open
28 (34)	MUTE	—		Audio output mute. Mute OFF at 1.5V or less Mute ON at 2.5V or more Mute OFF when open

Electrical Characteristics

(Ta=25°C, Vcc=9V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Icc	Vcc=9V, no signal, no load	41	51	66	mA

(Video system)

Gain	GVv	f=100kHz, 0.3Vp-p input (Fig. 1)	5.5	6.0	6.5	dB
Frequency response characteristics	FBWV1	0.3Vp-p input, input frequency where output amplitude is –3dB with 100kHz output serving as 0dB (Fig. 1)	15	20	—	MHz
Frequency response characteristics (Y/C mix)	FBWV2	0.3Vp-p input, input frequency where output amplitude is –3dB with 100kHz output serving as 0dB (Fig. 1)	10	15	—	MHz
Input dynamic range	Vdv	f=100kHz, maximum with distortion < 1.0% (Fig. 1)	2.0	—	—	Vp-p
Cross talk	Vctv	f=4.43MHz, 1Vp-p input (Fig. 2)	—	—	–50	Vp-p

(Audio system)

Gain	GVA	f=1kHz, 1Vp-p input, 6kΩ resistor inserted to input (Fig. 3)	–1	0	1	dB
Frequency response characteristics	FBWA	1Vp-p input, input frequency where output amplitude is –3dB with 100kHz output serving as 0dB (Fig. 3)	50	—	—	kHz
Total harmonic distortion	THD	f=1kHz, 2.2Vp-p input, when 400Hz HPF+80kHz LPF are inserted (Fig. 3)	—	0.03	0.05	%
Input dynamic range	VdA	f=1kHz, maximum with distortion < 0.3 % (Fig. 3)	2.8	3.0	—	Vrms
Cross talk	VctA	f=1kHz, 1Vp-p input (Fig. 4)	—	–90	–80	dB
Ripple rejection ratio		f=100Hz, 0.3Vp-p applied to Vcc (Fig. 5)	—	–55	–40	dB
Output DC offset	VOFF	Offset voltage between input and output (Fig. 6)	–30	—	30	mV
Residual noise	VNA	fCL=300Hz, fCH=19kHz, 40dB amplifier connected (Fig. 7)	0	—	6.0	mV
S/N ratio	S/N	f=1kHz, 1Vrms input (Fig. 3)	90	100	—	dB

(Logic system)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		3.0	—	5.0	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA 3mA current supplied	0	—	0.4	V
High level input current	I_{IH}	V_{IH}=4.5V	0	—	10	µA
Low level input current	I_{IL}	V_{IL}=0.4V	0	—	10	µA
Maximum clock frequency	f_{SCL}		0	—	100	kHz
Minimum waiting time for data change	t_{BUF}		4.0	—	—	µs
Minimum waiting time for data transfer start	$t_{HD;STA}$		4.0	—	—	µs
Low level clock pulse width	t_{LOW}		4.7	—	—	µs
High level clock pulse width	t_{HIGH}		4.0	—	—	µs
Minimum waiting time for start preparation	$t_{SU;STA}$		4.7	—	—	µs
Minimum data hold time	$t_{HD;DAT}$		0	—	—	s
Minimum data preparation time	$t_{SU;DAT}$		250	—	—	ns
Rise time	t_R		—	—	1	µs
Fall time	t_F		—	—	300	ns
Minimum waiting time for stop preparation	$t_{SU;STO}$		4.7	—	—	µs

Electrical Characteristics Measurement Circuit

* Parenthesized numbers indicate Pin No. of CXA1855S.

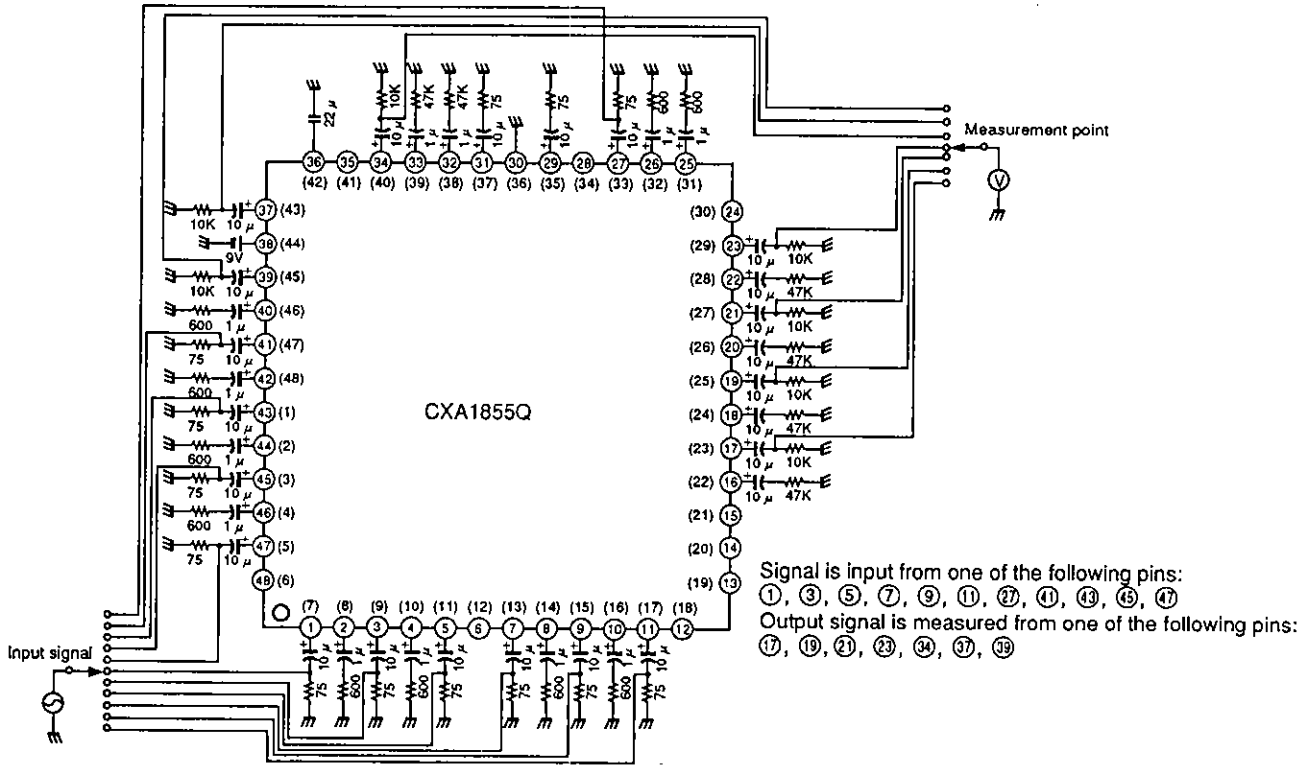


Fig 1. Video system (gain, frequency response characteristics, input dynamic range)

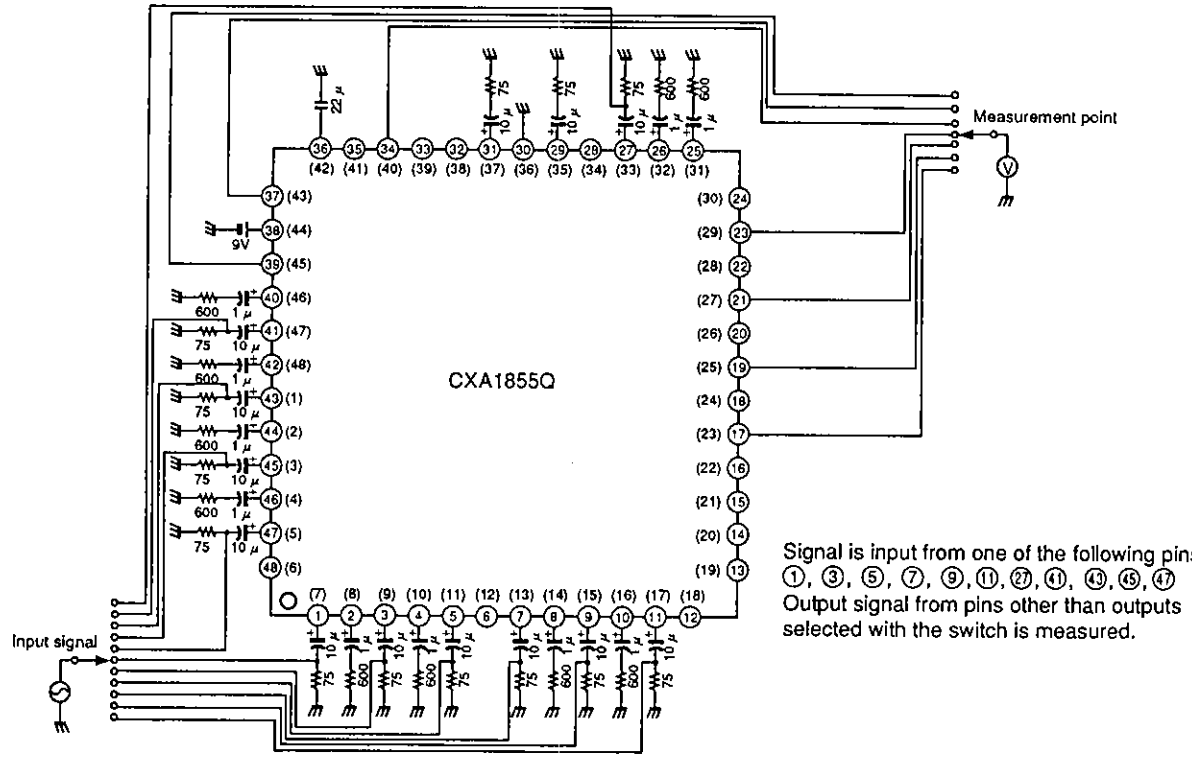


Fig 2. Video system (cross talk)

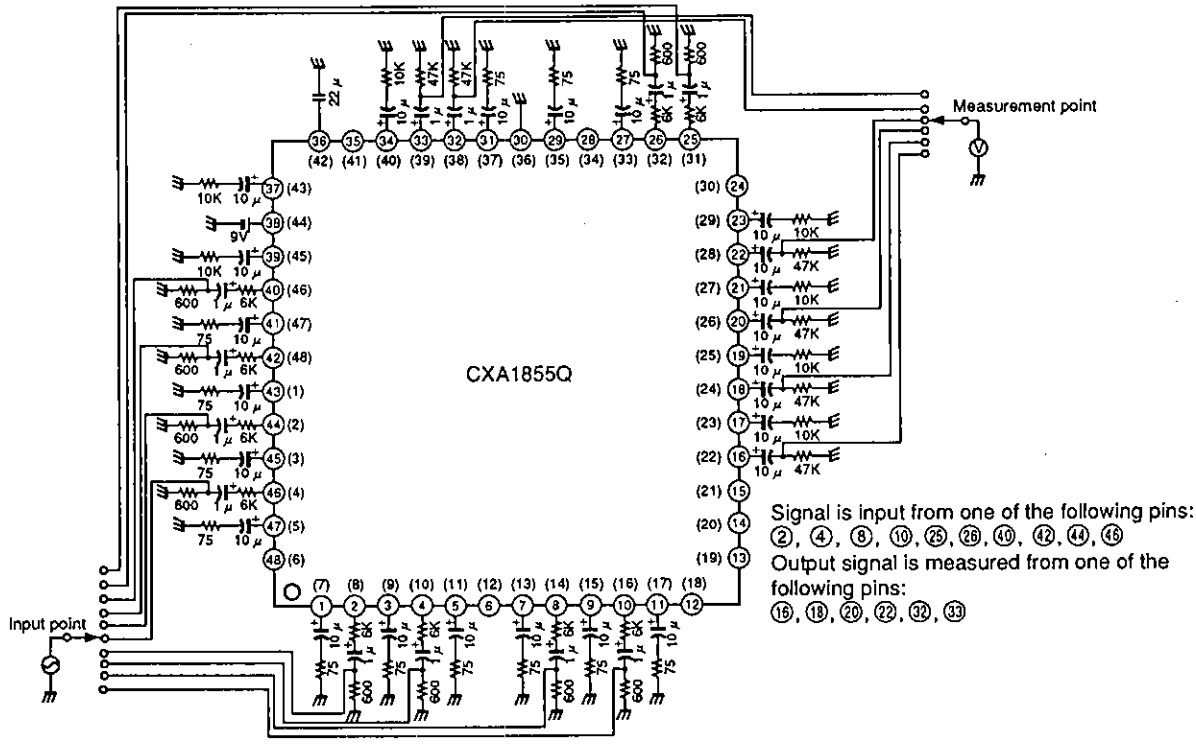


Fig 3. Audio system
(gain, frequency response characteristics, total harmonic distortion, input dynamic range)

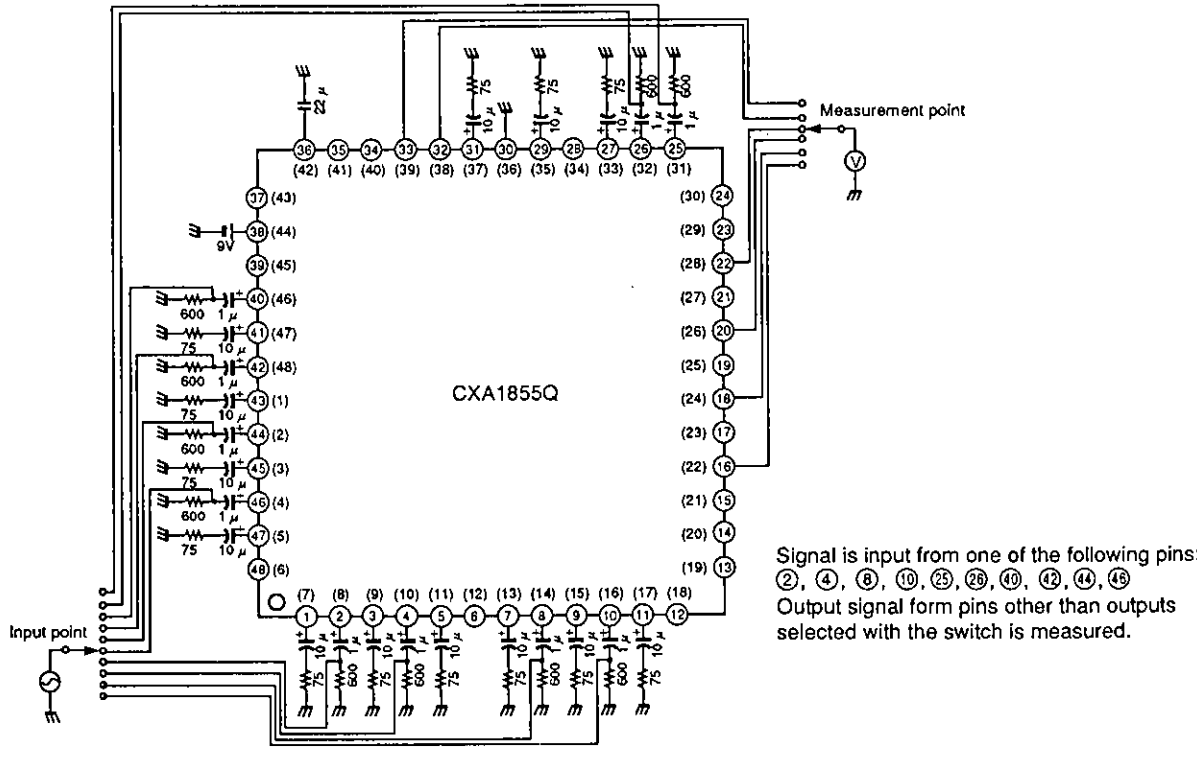


Fig 4. Audio system (cross talk)

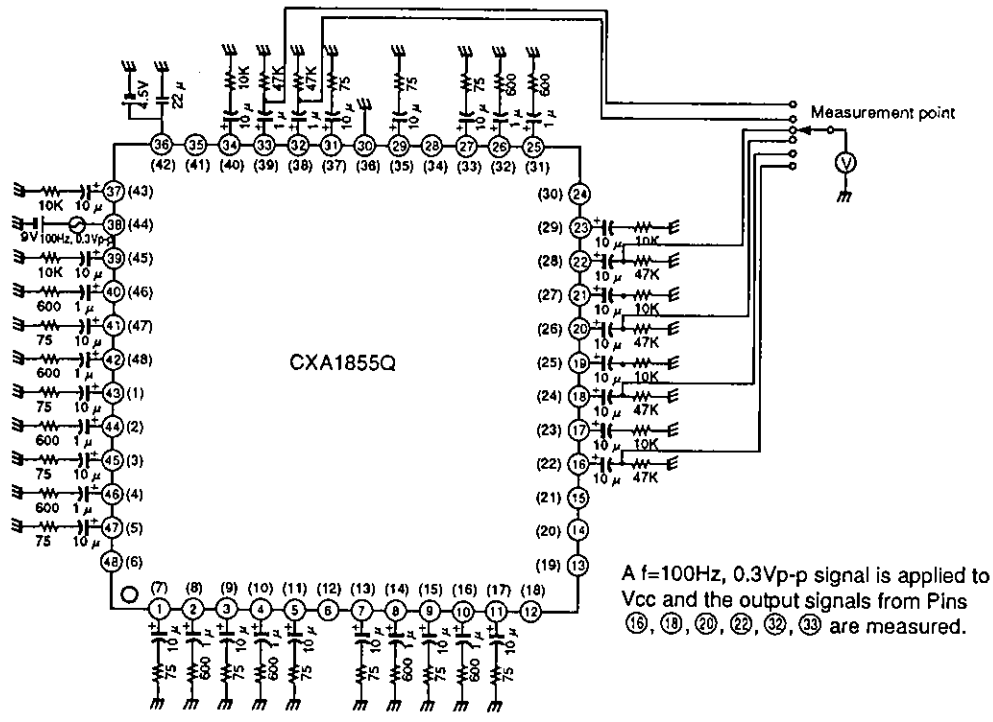


Fig 5. Audio system (ripple rejection)

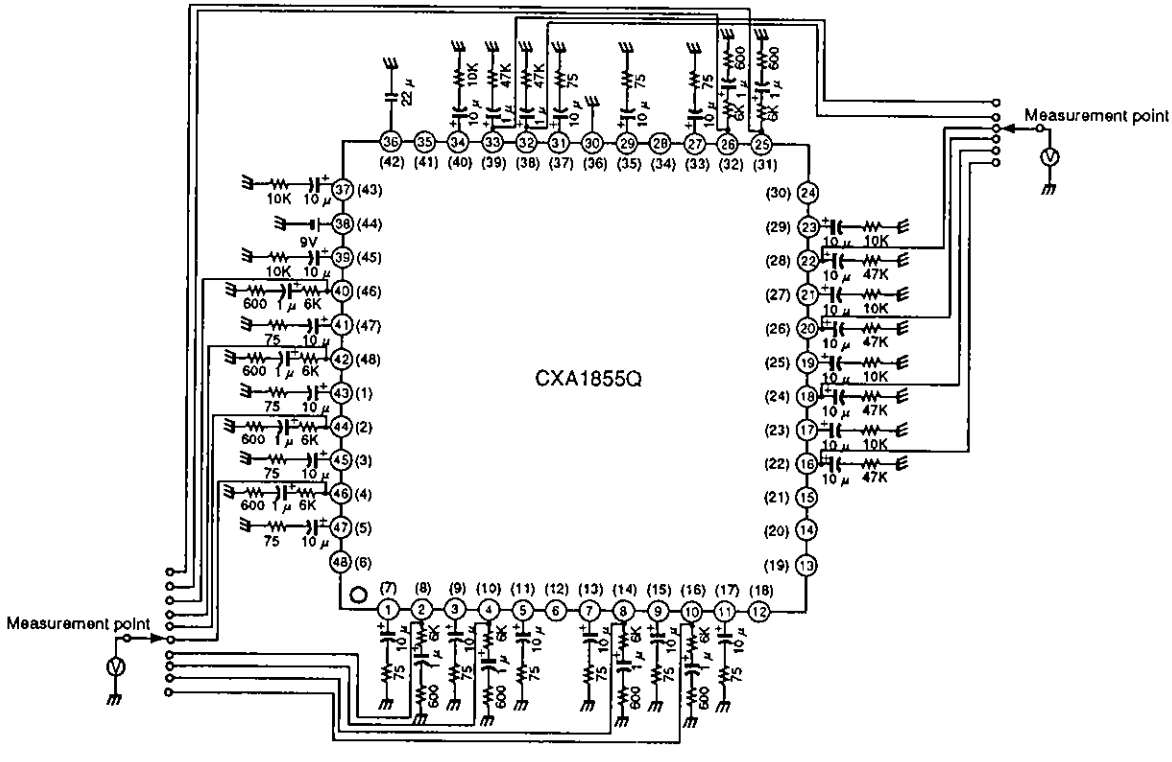


Fig 6. Audio system (output DC offset)

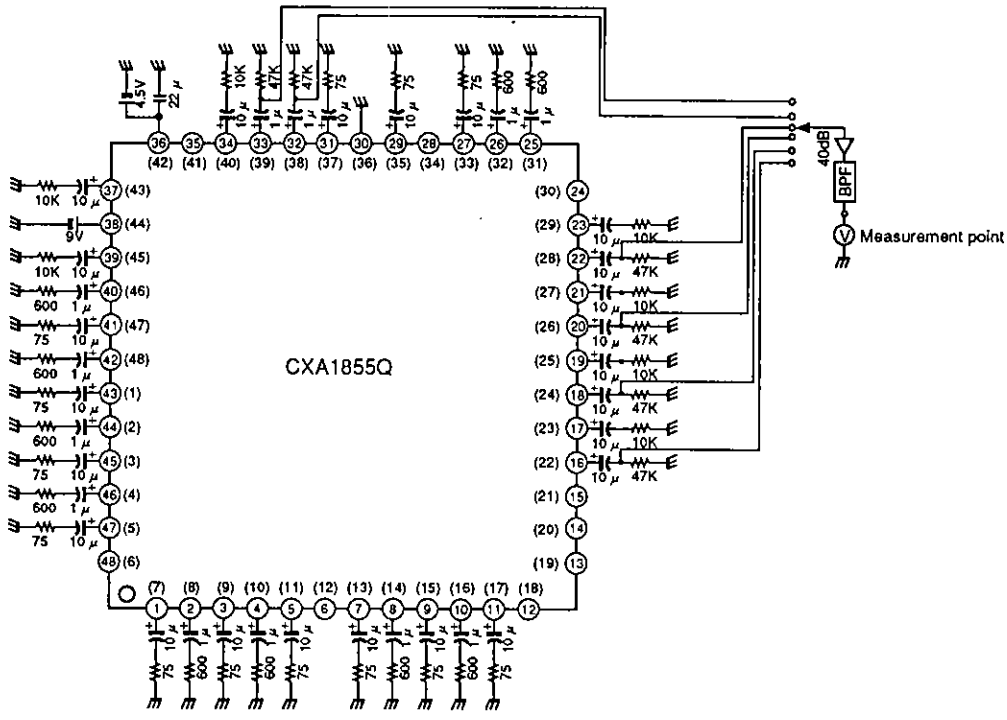
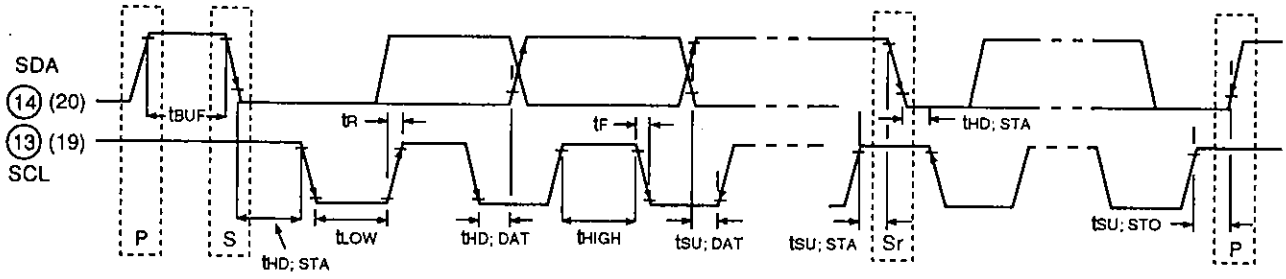


Fig 7. Audio system (residual noise)

I²C Bus Control Signal



* Parenthesized numbers indicate Pin No. of CXA1855S.

Fig 7.

Description of Operation

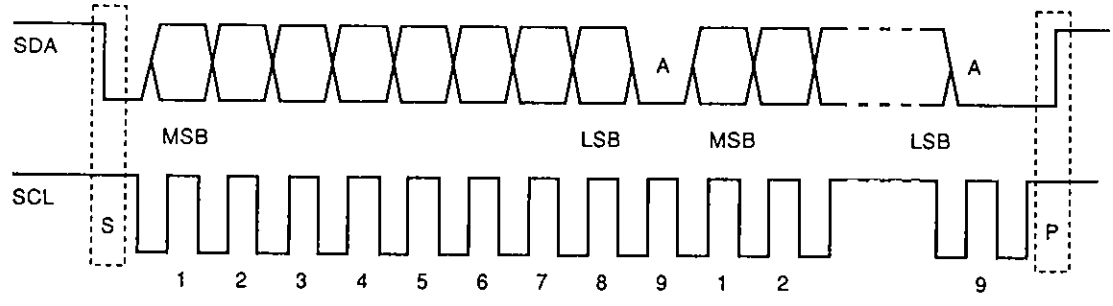
The CXA1855Q/S is a TV I²C bus-compatible AV switch IC. The video system and the stereo audio system both have 5 inputs and 3 outputs each. Each video output is provided with a built-in 6dB amplifier. Desired inputs can be independently assigned to all outputs (in the audio system, the left and right channels are processed as one unit) by I²C bus control.

I²C Bus Registers

(1) I²C Bus

The I²C bus (Inter-IC bus) is an inter-IC bus system developed by Phillips.

Two wires (SDA-serial data, SCL-serial clock) provide control over start, stop, data transfer, synchronization, and collision avoidance. The IC outputs are either open collector or open drain, forming a bus line in the wired OR format.



S: Start condition; SDA is set at "Low" when SCL is "High"
P: Stop condition; SDA is set at "High" when SCL is "High"
A: Acknowledge signal sent from the slave

Data is transmitted by MSB-first. One data unit consists of 8 bits, to which the acknowledge signal, which indicates that the data has been accepted by the slave, is attached at the end. Normally, the slave*1 IC receives data at the rising edge of SCL and the master*2 IC changes data at the falling edge of SCL.

*1 Slave: An IC that is placed under the control of the master. In a normal system, all devices excluding the central microcomputer are slaves.

*2 Master: A central microcomputer or other controlling IC.

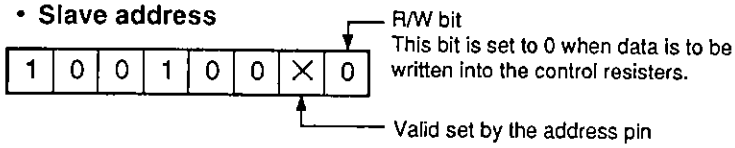
(2) Control Registers

The CXA1855Q/S control is exercised by writing 3-byte data into the three 8-bit control registers which control the 3 outputs selector circuits.

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	P

S: Start condition
A: Acknowledge
P: Stop condition

• **Slave address**



DATA1 Provides video 1 output control
DATA2 Provides video 2 output control
DATA3 Provides video 3 output control

• **Control register structure (DATA1 to DATA3)**

b7 b6	b5 b4 b3	b2 b1 b0
S-CONT (2)	VIDEO (3)	AUDIO (3)

Parenthesized numbers indicate the number of bits

Each register is set to 0 upon power ON.

Video switch control (VIDEO)

b5	b4	b3	Input signal selected
0	0	0	Mute
0	0	1	TV
0	1	0	1V system
0	1	1	2V system
1	0	0	3V system
1	0	1	EV

Others-Mute

1V system: V1, Y1, C1
2V system: V2, Y2, C2
3V system: V3, Y3, C3

Audio switch control (AUDIO)

b2	b1	b0	Input signal selected
0	0	0	Mute
0	0	1	RTV/LTV
0	1	0	RV1/LV1
0	1	1	RV2/LV2
1	0	0	RV3/LV3
1	0	1	REV/LEV

Others-Mute

S input control (S CONT)

b7	b6	Output pin
1	0	Selects the composite input
1	1	Selects the S input

Composite input: TV, V1, V2, V3, EV
S input: Y1, C1, Y2, C2, Y3, C3

Note) The YOUT1 and COUT1 switches are also switched by this control.

(3) Status Registers

S	Slave address	A	DATA	NA	P

S: Start condition
P: Stop condition
A: Acknowledge

When communication is to be terminated in the status register reading mode, the "no acknowledge" signal is needed to assure that the master does not issue the acknowledge signal to slave.

• **Slave address**

1	0	0	1	0	0	X	1

R/W bit
This bit is set to 1 when the status register is to be read.

Value set by the address pin

• **DATA**

b7	b6	b5	b4	b3	b2	b1	b0
PONRES	X	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	S3 OPEN	S3 SEL

PONRES

When the CXA1855Q/S is reset upon power ON, logical 1 is returned. Once a read operation is completed, logical 0 is returned.

S1 to S3 OPEN
0: S1 to S3 pins are not open.
1: S1 to S3 pins are open.

S1 to S3 SEL
0: S1 to S3 pins are not grounded.
1: S1 to S3 pins are grounded.

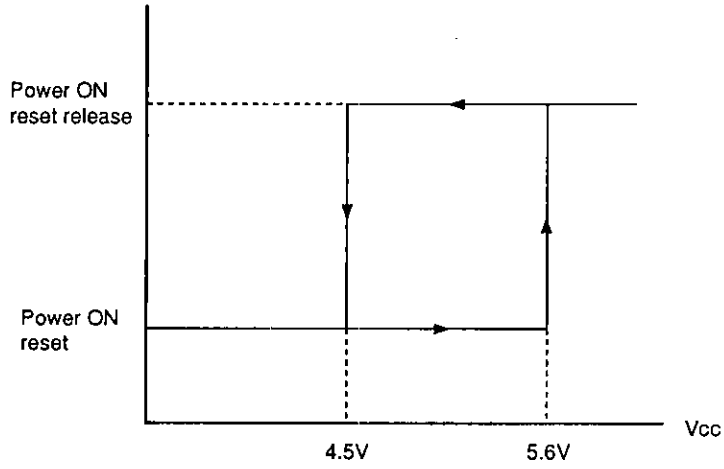
In actually, the logic states of the S1 to S3 OPEN and the S1 to S3 SEL bits are determined by comparing the DC voltages of S1 to S3 pins to two threshold values.

DC voltage of S1 to S3 pins	S1 to S3 OPEN	S1 to S3 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

(4) Power ON reset

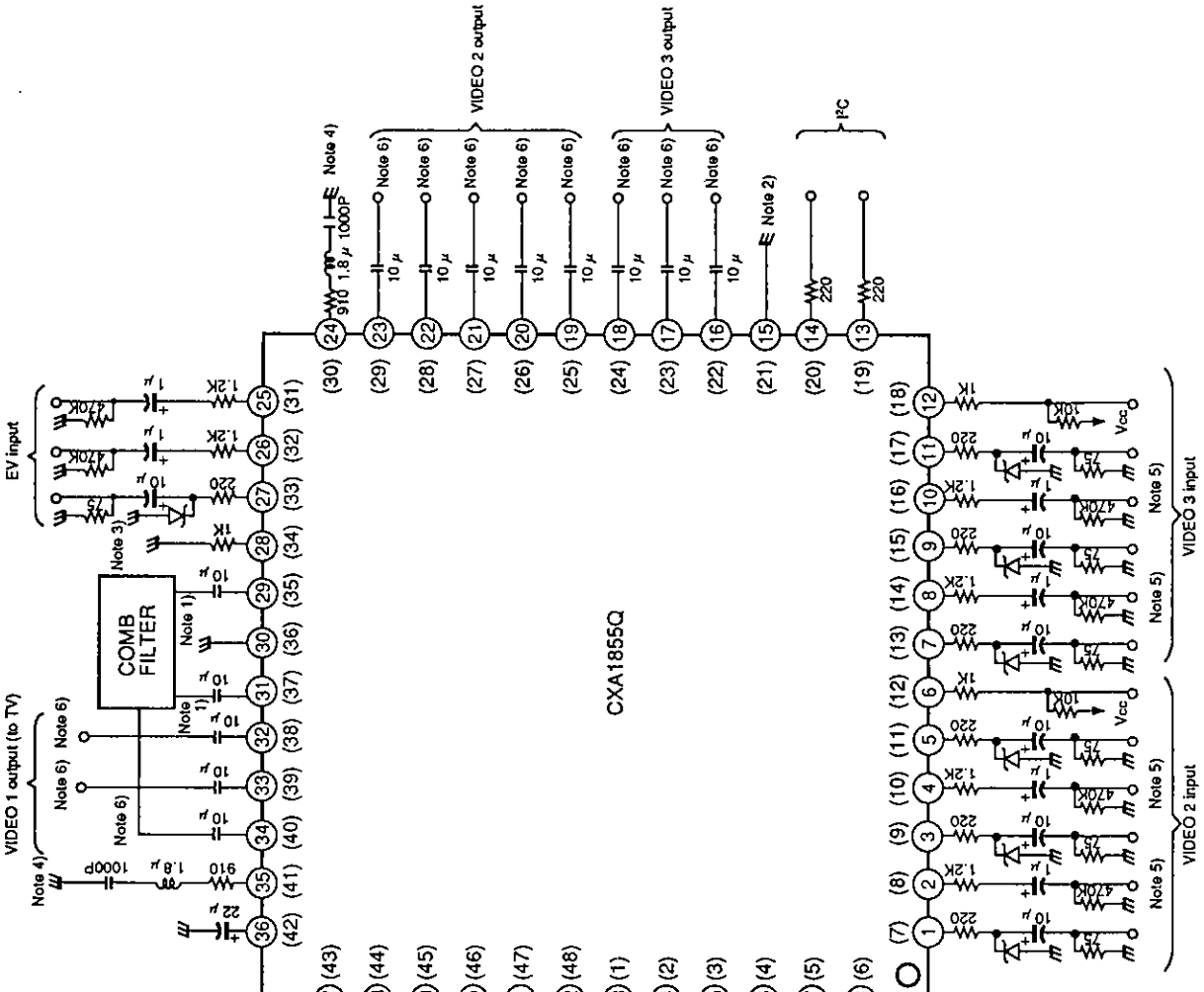
The CXA1855Q/S incorporates the power ON reset function. Therefore, each control register is reset to 0 upon power ON. The power ON reset Vcc and released Vcc are as shown below.

The power ON reset V_{TH} is hysteretical. The PONRES bit of the status register is read to determine whether the IC is reset upon power ON.



Application Circuit

* Parenthesized numbers indicate Pin No. of CXA1855S.



Note 1) Depending on the output bias of the comb filters, pay attention to the polarities of the capacitors since the bias at Pins ㉙ and ㉛ is approximately 4.5V.

Note 2) Connect Pin ⑮ to Vcc when setting the slave address of the IC to 92H.

Note 3) The audio output can be muted by setting Pin ㉘ to 3.5V or more.

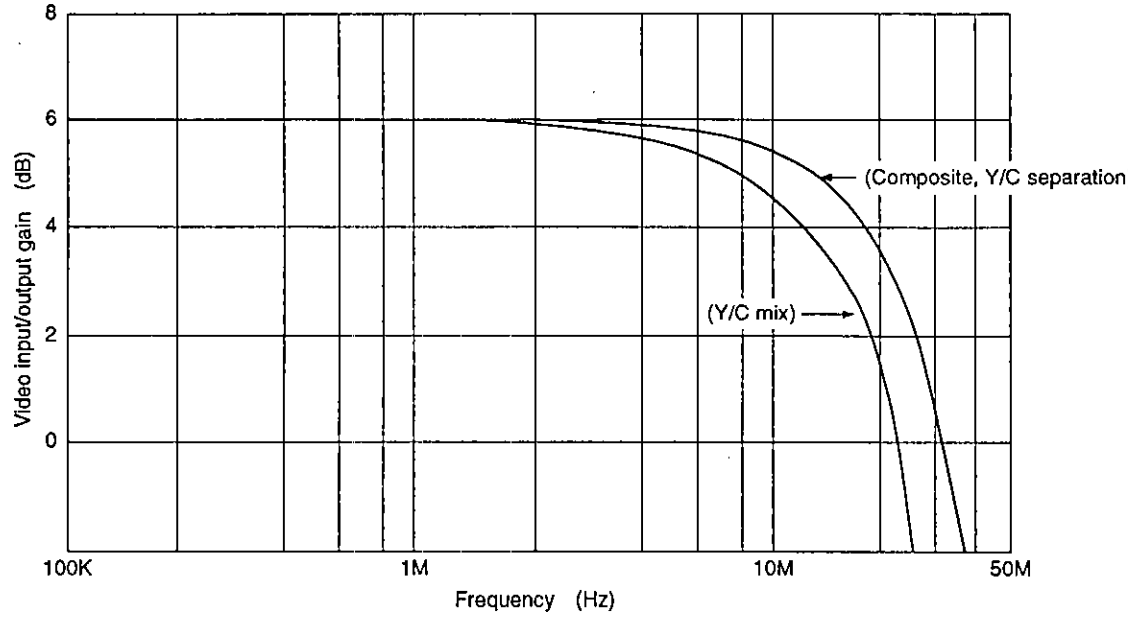
Note 4) The traps (Pins ㉔ and ㉟) are of 3.58MHz subcarrier. Attenuation is 6dB for 910Ω resistor.

Note 5) The output impedance of the audio signal source must be 4.7kΩ.

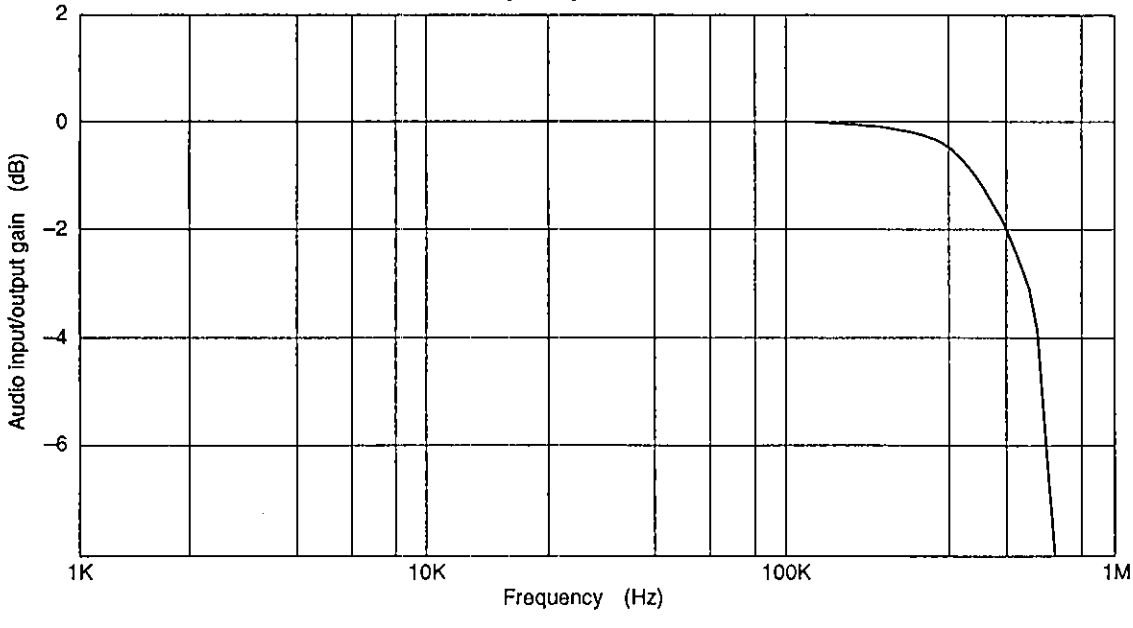
Note 6) Pay attention to the polarities of the capacitors since the bias at Pins ⑯, ⑰, ⑱, ⑲, ⑳, ㉑, ㉒, ㉓, ㉜, ㉝, ㉞, ㊲ and ㊳ is between 4.5V and 4.6V.

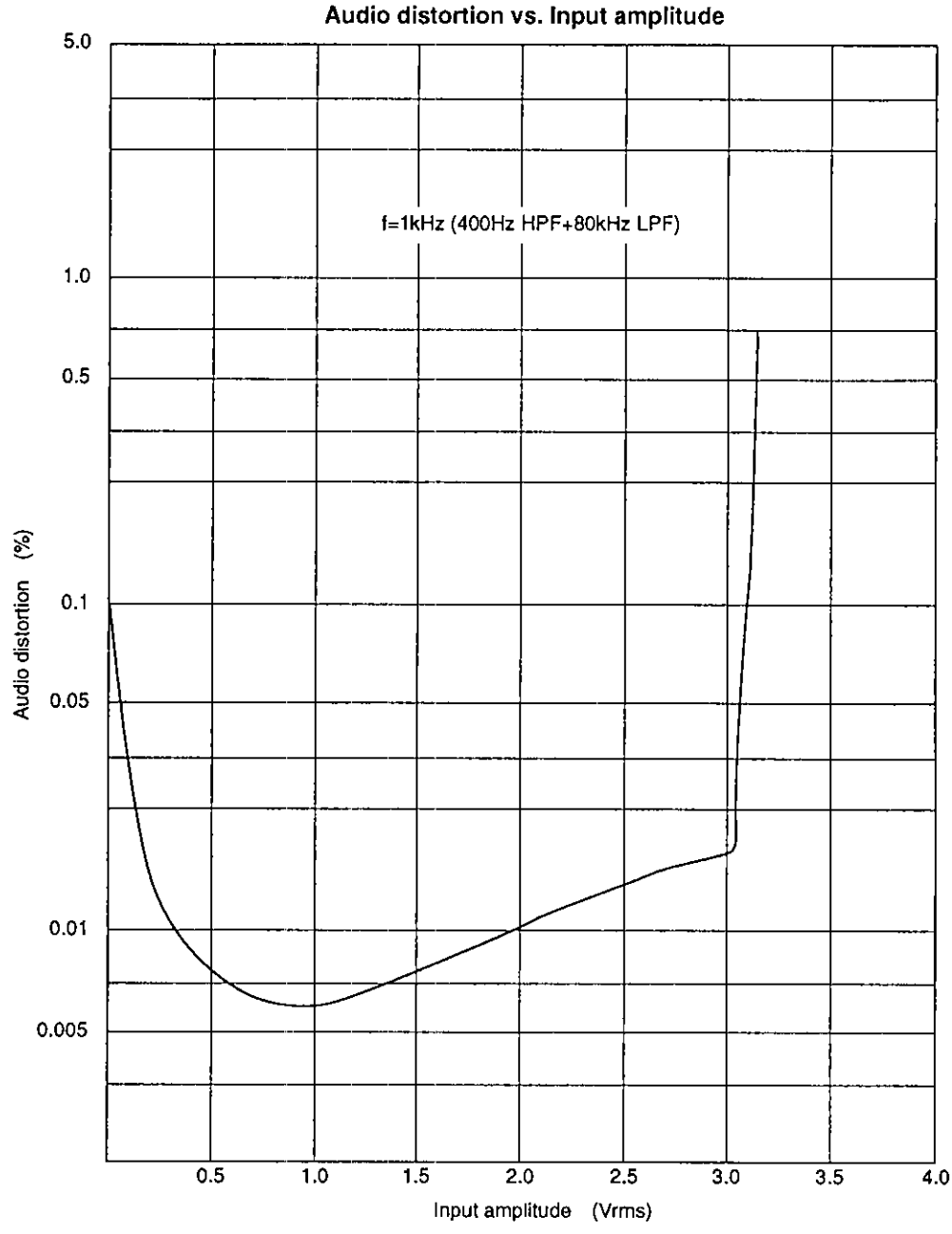
Example of Representative Characteristics

Video frequency characteristics



Audio frequency characteristics



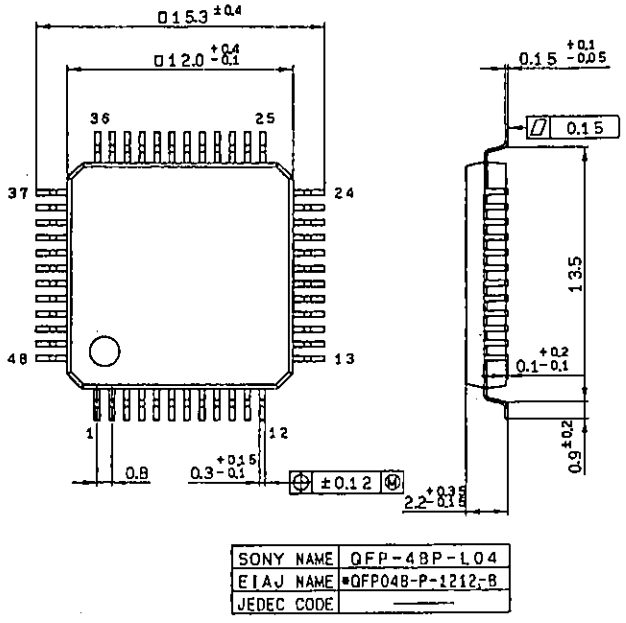

Audio distortion vs. Input amplitude
f=1kHz (400Hz HPF+80kHz LPF)
Audio distortion (%)
5.0
1.0
0.5
0.1
0.05
0.01
0.005
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Input amplitude (Vrms)

Package Outline

Unit : mm

CXA1855Q

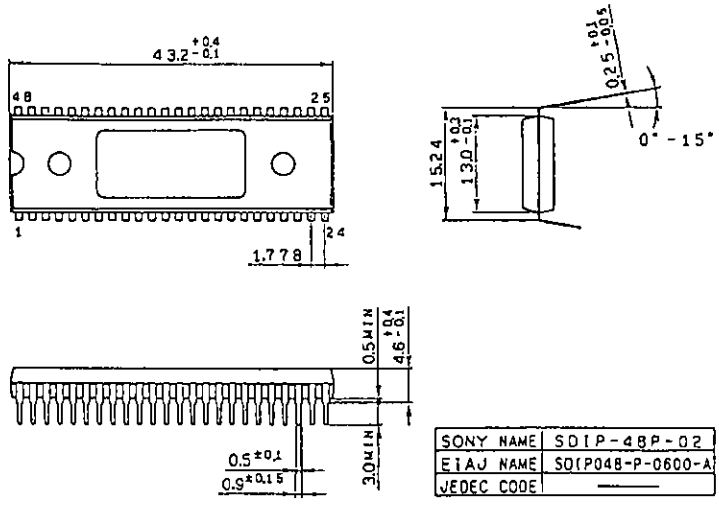
48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

CXA1855S

48pin SOIP (Plastic) 600mil 5.1g



SONY NAME	SOIP-48P-02
EIAJ NAME	SOIP048-P-0600-A
JEDEC CODE	———