uPD1719G

Internal Prescaler, PLL Synthesizer, and LCD driver Microcontroller

The uPD1719G is a 4-bit CMOS microcontroller with prescaler that can input up to 150 MHz, PLL synthesizer, and 1/2 duty, 1/2 bias LCD dirver.

The 4-bit CPU execute arithmetic operations (AD and SU), boolean operations (EXL), bit test (TMT), carry flag set reset instruction (STC), and timer function.

The 24 I/O ports are controlled by IN and OUT instructions. The serial I/O , 6 bit A/D converter, and clock generator port are controlled by special instructions.

The 16-bit IF counter can input FM/AM IF to detect a valid station during auto tuning.

Features:

1. 4-bit microcontroller for digital tunning
2. Two modulus prescaler : 150 MHz max.
3. Power supply 5 V +/- 10%
4. CMOS process
5. Power down mode (by CE terminal)
6. Program memory (ROM) 16-bit X 2040 steps
7. Data memory (RAM) 4-bit X 256 word
8. Instruction set : 93
9. Instruction cycle time : 33.3 us (4.5 MHz crystal)
10. Arithmetic intructions (12 addition and 12 subtraction)
11. Conditional instruction (AIS <- -> AIN)
12. Data transfer within the same row
13. Data transfer with the registers. (MVRD, MVRS)
14. 16 general purpose registers.
15. Stack level : 3 levels

16. LCD driver (1/2 duty, 1/2 bias, frame frequency : 100 Hz)

17. User programmable PLA for LCD display pattern

18. Power down mode by stopping the clock. (CKSTP)

19. 8 I/O port (PA3 - PA0 : individual pin can be selected
PC3 - PC0 : 4 bits can be selected either input or output

20. 12 output ports (PB3 - PB0, PD3 - PD1, CGP, PL3 - PL0
PL3 - PL0 share pins with LCD segment drivers)

21. Internal serial interface (PA3/SCK : shift clock,
PA2/SI, serial in, PB0/SO : serial output)

22. 6 bit A/D converter (Vref = VDD : conversion is
executed in software by TADT and TADF instructions)

23. Clock generator port (Signal Generator (SG) : 180 KHz
or 18 KHz are divided in 64 steps. Variable Duty Port
(VDP) : the duty of 2.69 KHz is changed in 64 steps)

24. LCD segment driver and key matrix signal source share
common ports.

25. Key input port (K3 - K0)

26. I/O instructions (IN and OUT)

27. Port status test (TPT and TPF)

28. External edge triggerd interrupt

29. IF counter (Gate duration : 1 ms, 4 ms, 8 ms, infinity
Maximum input freq. : FMIF = 12 MHz, AMIF= 1 MHz)

30. 125 ms interval timer and timer F/F

31. Internal 5 ms 60 % duty clock

32. PLL lock status test (TUL)

33. PLL dividing number loaded and the PLL method selected
by one instruction (PLL)

34. Direct connection of FM and AM signals from VCO
(max : AM = 15 MHz, FM = 150 MHz)

35. Pulse swallowing method and direct method can be
software selected.

36. Two error out terminal (EO1, EO2)

37. 7 reference frequencies (1 KHz, 5 KHz, 6.25 KHz, 9 KHz,
10 KHz, 12.5 KHz, 25 KHz)

38. Hardware support :

EVAKIT	***	EVAKIT-1700 + EV-1714
SE board	***	SE-1700 + EV1714 *1

39. software support : MP/M-86, CP/M base cross assembler

(uS281AS1700, uS171AS1700)

*1 MP/M-86, CP/M are trademark of Digital Research

Absolute Maximum Ratings

parameter	symbol	rating	units
Supply Voltage	VDD	-0.3 to +6.0	V
Input Voltage	VI	-0.3 to +VDD	V
Output Voltage	VO	-0.3 to +VDD	V
Output absorbing current	IO	10	mA
Storage temperature	Tstg	-55 to +125	C
Operating temperature	Topt	-40 to +85	C

Recommended Operating Conditions

parameter	symbol	conditions	MIN	TYP	MAX	units
PLL operating	VDDP	VDD1	4.5	5	5.5	V
CPU operating	VDDC	PLL stopped	3.8	5	5.5	V
Data retention	VDDR	crystal stopped	2.5		5.5	V

Electrical Characteristics (Ta = -40 to +85 C, VDD 4.5 to 5.5V)

paramerer	symbol	conditions	MIN	TYP	MAX	units
High level input voltage	VIH1	PORT A, C	0.7*VDD			V
High level input voltage	VIH2	CE, $\overline{INT}$	0.8*VDD			V
High level input voltage	VIH3	K3 - K0	0.6*VDD			V
Low level input voltage	VIL1	PORT A, C			0.2*VDD	V
Low level input voltage	VIL2	K3 - K0, CE, $\overline{INT}$			0.2*VDD	V
High level output current	-IOH1	Port A, B, C, D VOH = VDD - 0.4 v	0.4			mA
High level output current	-IOH2	EO1,EO2,CGP,PL3-PL0 VOH = VDD - 1 V	0.5			mA
High level output current	-IOH3	S0 - S23 VOH = VDD - 1V	10	18		uA
Low level output current	IOL1	PORT A, B, C, D, CGP PL3-PL0 VOL = 0.4 V	0.6			mA

parameter	symbol	conditions	MIN	TYP	MAX	UNIT
Low level output current	IOL2	EO1, EO2 VOL = 1 V	0.5			mA
Low level output current	IOL3	S0 - S23 VOL = 1 V	10	30		uA
High level input current	IIH1	K3 - K0 VI = VDD = 4.5 V	15		150	uA
High level input current	IIH2	VCOH, VCOL, XI VI = VDD = 4.5 V	100			uA
Output voltage	VCOM1	COM0, COM1 VDD = 5 V, output open	4.8	5.0		V
Output voltage	VCOM2	COM0, COM1 VDD = 5 V, output open	2.3	2.5	2.7	V
Output voltage	VCOM3	COM0, COM1 VDD = 5 V, output open	0	0.2		V
Output off leak current	IL	EO1, EO2 VO = VDD, TA = 25 C		1 nA	1uA	A
Input frequency	fIN1	VCOH Vi = 0.5 Vp-p	15		150	MHz
Input frequency	fIN2	VCOH Vi = 0.3 Vp-p	15		130	MHz
Input frequency	fIN3	VCOL Vi = 0.5 Vp-p	0.6		15	MHz
Input frequency	fIN4	PA1/FMIF Vi = 0.5 Vp-p			12	MHz
Input frequency	fIN5	PA0/AMIF Vi = 0.5 Vp-p			1	MHz
A/D resolution					6	bit
A/D error		Topt = -10 to +50 C		1	1.5	bit
PLL operating current	IDDP	CPU and PLL operating fIN = 150 MHz VDD = 5 V, Ta = 25 C		15		mA
CPU operating current	IDDC	PLL disabled CPU oper. VDD = 5 V, Ta = 25 C		0.5		mA
Data retention current	IDDR	Xtal off, Ta = 25 C , VDD=5V		10	150	nA

Pin Description

PIN #	Symbol	Pin Name	Description
1	NC	No-Connection	
2 3	EO1 EO2	Error Outputs	This is the PLL error out terminals. If the freq. of divided VCO is greater than the reference a high level is output. If lower then a low level is output. The EO pin will float if both are equal.
26,58	GND	Ground	The ground terminal of the device
5	VCOL	local osc signal input low	This terminal receives the local osc outputs (VCO output) from 0.6 to 15 MHz (0.3 Vp-p MIN). Using the direct method 16 to (2 expl2 - 1) division can be made. During pulse swallowing method this pin is pulled down to ground
6	VCOH	local osc signal input	This terminal receives the local osc outputs (VCO output) from 15 to 150 MHz (0.5 Vp-p MIN). Using the pulse swallowing method 1024 to (2 expl2 - 1) division can be made.
7	CE	Chip enable	This is the device select terminal. When this pin is high level, the device operates normally, PLL operational. When this pin is low level, the CPU is operational but the PLL is disabled. Any input less than 134 uS will not be acceptable. If CKSTP instruction is executed when CE is in low state, the CPU stops and the device will enter the data retention mode. During this power down mode (10 uA typical) the LCD driver is disabled. If CE is in high state then the CKSTP instruction will be treated as a NOP. During the low to high transition of CE line the device is reset and the PC is reset to 0. PORT A, C are set to input.
9 | 11	PD1 | PD3	PORT D	3 bit output port *note 1, 3

12 | 15	PC3 | PC0	PORT C	4-bit input output port. If OUT, SPB, or RPB instruction is used it will be output port. If IN instruction is used then it will be input port. *note 1, 2, 3
16 17 18 19	PA0/AMIF PA1/FMIF PA2/SI PA3/SCK	PORT A	4-bit input port. The direction of individual pin is determined by the content of 1FH of BANK0. When the device is reset this port becomes input port. PORT A shares pins with serial I/O. The serial data in and shift clock are common with PA2 and PA3. PA0 and PA1 can be used for IF counters. The AMIF can input up to 1 MHz and the FMIF can input up to 12 MHz. The AMIF is directly fed to the IF counter FMIF is divided by 2 before the signal is fed to the IF counter. * note 1, 2
20 | 23	PB3 | PB0/SO	PORT B	4 bit output port PB0 is used as serial data out pin when SIO instruction is executed. * note 1, 3
24 25	XO XI	Crystal	4.5 MHz crystal is connected to this terminal.
4 8	VDD	Power Supply	This is the device power supply. (5 V +/- 10 %) During the data retention mode (CE low and CKSTP executed) VDD can be lowered to 2.5 V. When this terminal's voltage is raised from 0 V to 4.5 V the device is reset and the PC is reset to 0. Pin 26 and pin 58 are internally connected, therefore it is not neccessary to apply power to both pins.
27	CGP	Clock Generator port	This terminal is the clock generator port or 1 bit output port selected in software. If this pin is used as CGP it can be used as a variable duty port or signal generator port. The duty of 2.69 KHz is changed by 64 steps during the VDP mode. If SG mode is selected the frequency can be changed 64 steps using 18 KHz or 180 KHz as the reference. When the device is reset the CGP pin is low level. * note 1

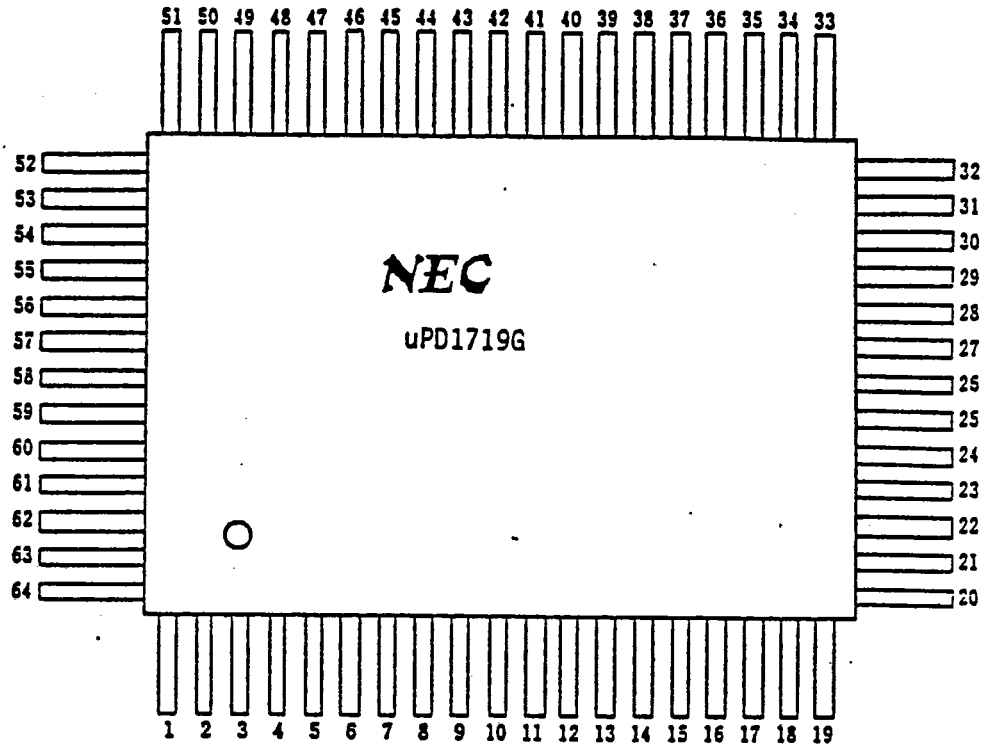
28 | 55	S27 | S0	LCD segment outputs	56 dots can be displayed and controlled by the segments and COM0 COM1 matrix. S27/PL3 - S24/PL0 can be used as 4 bit output port when not used for LCD segment driver. S15/KS15 - S0/KS0 can be used for key matrix source signal. * note when device is reset display will be off mode.
56 57	COM0 COM1	LCD Common Outputs	100 Hz 1/2 duty signal is output via this terminal
59 | 62	K3 | K0	Key Return signal input	This is the 4 bit key input port. When KIN or KI instruction is executed the key data is stored in specified RAM location.
63	AD	Analog Digital Input	A/D converter input. The conversion is made in software so that you have the option of 6-bit to 1-bit resolution.
64	INT	Interrupt	When falling edge is detected the program counter is set to location 1.

* note 1 When IN, OUT, SPB, RPB instructions are executed PA0 is LSB and PA3 is MSB. PORT B and PORT C are also same as PORT A.

* note 2 When the device is reset (VDD low -> high) or CKSTP is is executed, PORT A and PORT C are set to input mode.

* note 3 PORT B and PORT D data will be indeterminate when device is reset (VDD low -> high). Therefore they must be initialized by the program. When CS low -> high or during CKSTP the output data will not change.

(Top View)

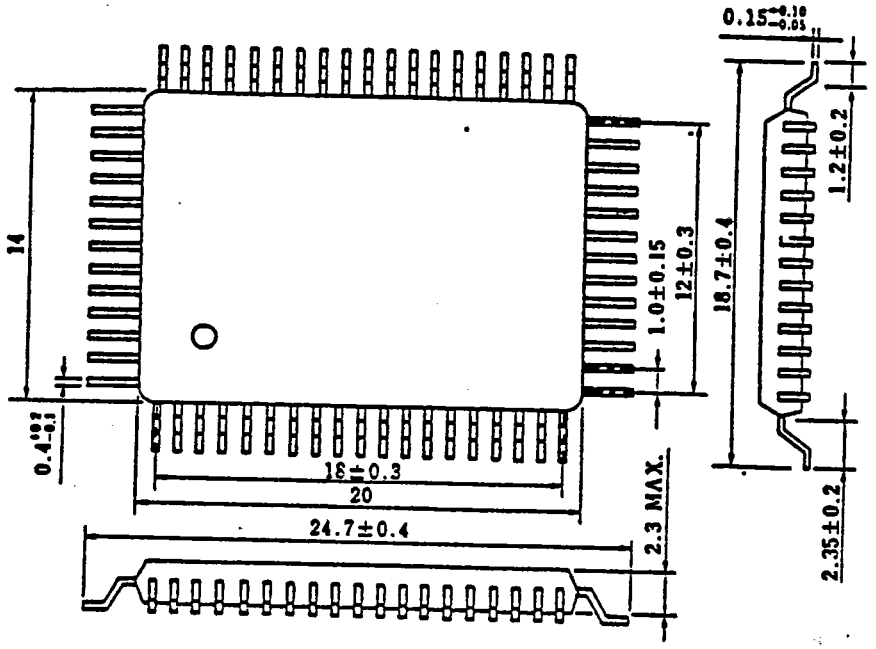


pin#	Symbol	pin#	symbol	pin#	symbol	pin#	symbol
1	NC	17	PA1/FMIF	33	S22	49	S6/KS6
2	EO1	18	PA2/SI	34	S21	50	S5/KS5
3	EO2	19	PA3/$\overline{SCK}$	35	S20	51	S4/KS4
4	VDD	20	PB0/SO	36	S19	52	S3/KS3
5	VCOL	21	PB1	37	S18	53	S2/KS2
6	VCOH	22	PB2	38	S17	54	S1/KS1
7	CE	23	PB3	39	S16	55	S0/KS0
8	VDD	24	XO	40	S15/KS15	56	COM0
9	PD1	25	XI	41	S14/KS14	57	COM1
10	PD2	26	GND	42	S13/KS13	58	GND
11	PD3	27	CGP	43	S12/KS12	59	K3
12	PC0	28	S27/PL3	44	S11/KS11	60	K2
13	PC1	29	S26/PL2	45	S10/KS10	61	K1
14	PC2	30	S25/PL1	46	S9/KS9	62	K0
15	PC3	31	S24/PL0	47	S8/KS8	63	AD
16	PA0/AMIF	32	S23	48	S7/KS7	64	$\overline{INT}$

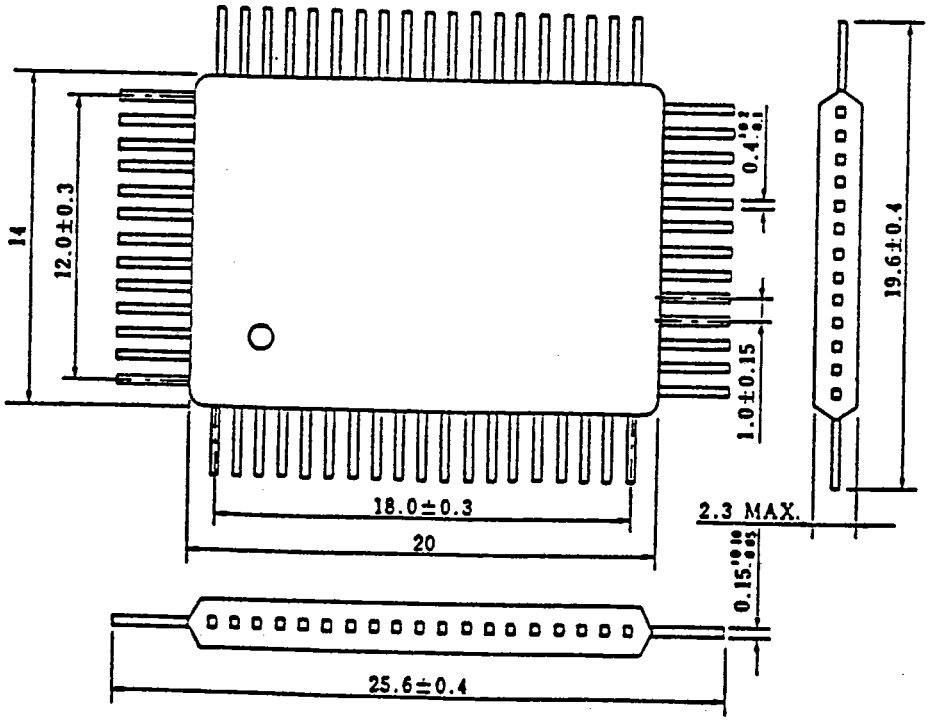
(NC : No Connection)

Package Dimensions (Unit : mm)

bent leads (12)



(11) straight leads



μPD1719G INSTRUCTION SET

μPD1719G Instruction Set Table

b_{13} b_{12} b_{11} b_{10}	b_{15} b_4	00	01	10	11
		0	1	2	3
0 0 0 0	0	SIO s IFCW w IFC t NOP	KIN M KI M	———	ST M, r
0 0 0 1	1	SPB P, N SS N_1 BANK1 BANK2 BANK3 EI STC	ORI M, I	———	MVRS M, r
0 0 1 0	2	JMP ADDR (page 1)	MVI M, I	OUT P, r	IN r, P
0 0 1 1	3	RPB P, N RS N_1 BANK0 DI RSC	ANI M, I	CKSTP HALT h	MVRD r, M
0 1 0 0	4	RT	AI M, I	MVSR M_1, M_2	AD r, M
0 1 0 1	5	RTS	SI M, I	EXL r, M	SU r, M
0 1 1 0	6	JMP ADDR (page 0)	AIC M, I	LD r, M	AC r, M
0 1 1 1	7	CAL ADDR (page 0)	SIB M, I	LCDD M, D	SB r, M
1 0 0 0	8	SBK0 P, N †PF N_2 †SF †CLF †TF †B0F †B1F	AIN M, I	†KLT †KLF †SFT †SFF †ADT †ADF	ADN r, M
1 0 0 1	9	†PT P, N †ST N_2 †CLT †TT †B0T †B1T	SIN M, I	TTM TIP TGC	SUN r, M
1 0 1 0	A	TMF M, N	AICN M, I	TUL	ACN r, M
1 0 1 1	B	TMT M, N	SIBN M, I	PLL M, r	SBN r, M
1 1 0 0	C	SLTI M, I	AIS M, I	SLT r, M	ADS r, M
1 1 0 1	D	SGEI M, I	SIS M, I	SGE r, M	SUS r, M
1 1 1 0	E	SEQI M, I	AICS M, I	SEQ r, M	ACS r, M
1 1 1 1	F	SNEI M, I	SIBS M, I	SNE r, M	SBS r, M

List of μPD1719G instructions

NOTE: D_H: Data memory address high (row address) (2 bits)
D_L: Data memory address low (column address) (4 bits)
Rn: Register number (4 bits)
I : Immediate data (4 bits)
N : Bit position (4 bits)
ADDR: Program memory address (10 bits)
—: All "1"
r : General register
One of addresses 00–0FH of BANK0
M : Data memory address
One of 00–3FH of BANK0 and 00–3FH of BANK1
P : Port 0≤P≤3

N_1 : Bit position of status word 1 $0 \leq N_1 \leq 0FH$
N_2 : Bit position of status word 2 $0 \leq N_2 \leq 0FH$
( ) : Contents of register of memory
c : Carry
b : Borrow
s : Data to S.M.R. $0 \leq s \leq 0FH$
w : Data to IF Controll Word $0 \leq w \leq 0FH$
t : Trigger conditions $0 \leq t \leq 3$
h : Halt release conditions $0 \leq h \leq 0FH$

	Mnemonic	Operand 1ST	Operand 2ND	Function	Operation	Machine code: Operation code			
Addition	AD	r	M	Add memory to register	r←(r)+(M)	110100	D_H	D_L	Rn
	ADS	r	M	Add memory to register, then skip if carry	r←(r)+(M) skip if carry	111100	D_H	D_L	Rn
	ADN	r	M	Add memory to register, then skip if not carry	r←(r)+(M) skip if not carry	111000	D_H	D_L	Rn
	AC	r	M	Add memory to register with carry	r←(r)+(M)+c	110110	D_H	D_L	Rn
	ACS	r	M	Add memory to register with carry, then skip if carry	r←(r)+(M)+c skip if carry	111110	D_H	D_L	Rn
	ACN	r	M	Add memory to register with carry, then skip if not carry	r←(r)+(M)+c skip if not carry	111010	D_H	D_L	Rn
	AI	M	I	Add immediate data to memory	M←(M)+I	010100	D_H	D_L	I
	AIS	M	I	Add immediate data to memory, then skip if carry	M←(M)+I skip if carry	011100	D_H	D_L	I
	AIN	M	I	Add immediate data to memory, then skip if not carry	M←(M)+I skip if not carry	011000	D_H	D_L	I
	AIC	M	I	Add immediate data to memory with carry	M←(M)+I+c	010110	D_H	D_L	I
	AICS	M	I	Add immediate data to memory with carry, then skip if carry	M←(M)+I+c skip if carry	011110	D_H	D_L	I
	AICN	M	I	Add immediate data to memory with carry, then skip if not carry	M←(M)+I+c skip if not carry	011010	D_H	D_L	I
Subtraction	SU	r	M	Subtract memory from register	r←(r)−(M)	110101	D_H	D_L	Rn
	SUS	r	M	Subtract memory from register, then skip if borrow	r←(r)−(M) skip if borrow	111101	D_H	D_L	Rn
	SUN	r	M	Subtract memory from register, then skip if not borrow	r←(r)−(M) skip if not borrow	111001	D_H	D_L	Rn
	SB	r	M	Subtract memory from register with borrow	r←(r)−(M)−b	110111	D_H	D_L	Rn
	SBS	r	M	Subtract memory from register with borrow, then skip if borrow	r←(r)−(M)−b skip if borrow	111111	D_H	D_L	Rn
	SBN	r	M	Subtract memory from register with borrow, then skip if not borrow	r←(r)−(M)−b skip if not borrow	111011	D_H	D_L	Rn
	SI	M	I	Subtract immediate data from memory	M←(M)−I	010101	D_H	D_L	I
	SIS	M	I	Subtract immediate data from memory, then skip if borrow	M←(M)−I skip if borrow	011101	D_H	D_L	I
	SIN	M	I	Subtract immediate data from memory, then skip if not borrow	M←(M)−I skip if not borrow	011001	D_H	D_L	I
	SIB	M	I	Subtract immediate data from memory with borrow	M←(M)−I−b	010111	D_H	D_L	I
	SIBS	M	I	Subtract immediate data from memory with borrow, then skip if borrow	M←(M)−I−b skip if borrow	011111	D_H	D_L	I
	SIBN	M	I	Subtract immediate data from memory with borrow, then skip if not borrow	M←(M)−I−b skip if not borrow	011011	D_H	D_L	I

	Mnemonic	Operand 1ST	Operand 2ND	Function	Operation	Machine code: Operation code			
Comparison	SEQ	r	M	Skip if register equals memory	r−M skip if zero	1 0 1 1 1 0	D_H	D_L	Rn
	SNE	r	M	Skip if register not equals memory	r−M skip if not zero	1 0 1 1 1 1	D_H	D_L	Rn
	SGE	r	M	Skip if register is greater than or equal to memory	r−M skip if not borrow (r)≧(M)	1 0 1 1 0 1	D_H	D_L	Rn
	SLT	r	M	Skip if register is less than memory	r−M skip if borrow (r)<(M)	1 0 1 1 0 0	D_H	D_L	Rn
	SEQI	M	I	Skip if memory equals immediate data	M−I skip if zero	0 0 1 1 1 0	D_H	D_L	I
	SNEI	M	I	Skip if memory not equals immediate data	M−I skip if not zero	0 0 1 1 1 1	D_H	D_L	I
	SGEI	M	I	Skip if memory is greater than or equal to immediate data	M−I skip if not borrow (M)≧I	0 0 1 1 0 1	D_H	D_L	I
	SLTI	M	I	Skip if memory is less than immediate data	M−I skip if borrow (M)<I	0 0 1 1 0 0	D_H	D_L	I
Logical operation	ANI	M	I	Logic AND of memory and immediate data	M←(M)∧ I	0 1 0 0 1 1	D_H	D_L	I
	ORI	M	I	Logic OR of memory and immediate data	M←(M)∨ I	0 1 0 0 0 1	D_H	D_L	I
	EXL	r	M	Exclusive OR Logic of memory and register	r←(r)⊕(M)	1 0 0 1 0 1	D_H	D_L	Rn
Transfer	LD	r	M	Load memory to register	r←(M)	1 0 0 1 1 0	D_H	D_L	Rn
	ST	M	r	Store register to memory	M←(r)	1 1 0 0 0 0	D_H	D_L	Rn
	MVRD	r	M	Move memory to destination memory referring to register in the same row	(D_H, Rn)←(M)	1 1 0 0 1 1	D_H	D_L	Rn
	MVRS	M	r	Move source memory referring to register to memory in the same row	M←(D_H, Rn)	1 1 0 0 0 1	D_H	D_L	Rn
	MVSR	M_1	M_2	Move memory to memory in the same row	(D_H, D_{L1})←(D_H, D_{L2})	1 0 0 1 0 0	D_H	D_{L1}	D_{L2}
	MVI	M	I	Move immediate data to memory	M← I	0 1 0 0 1 0	D_H	D_L	I
	PLL	M	r	Load N0−N3, N_F & memory to PLL registers	PLLR←(N0−N3), N_F & (M)	1 0 1 0 1 1	D_H	D_L	Rn
Bit test	TMT	M	N	Test memory bits, then skip if all bits specified are true	if M(N)=all "1", then skip	0 0 1 0 1 1	D_H	D_L	N
	TMF	M	N	Test memory bits, then skip if all bits specified are false	if M(N)=all "0", then skip	0 0 1 0 1 0	D_H	D_L	N
Jump	JMP	ADDR		Jump to the address specified in page 0	PC←ADDR, PAGE←0	0 0 0 1 1 0	ADDR(10 bits)		
				Jump to the address specified in page 1	PC←ADDR, PAGE←1	0 0 0 0 1 0			
Subroutine	CAL	ADDR		Call subroutine in page 0	Stack←((PC)+1, PAGE), PC←ADDR, PAGE←0	0 0 0 1 1 1	ADDR(10 bits)		
	RT			Return to main routine	PC←(stack)	0 0 0 1 0 0	−	−	−
	RTS			Return to main routine, then skip unconditionary	PC←(stack), and skip	0 0 0 1 0 1	−	−	−
Interrupt	EI			Enable interrupt	INTE F/F←1	0 0 0 0 0 1	−	0 0 0 1	−
	DI			Disable interrupt	INTE F/F←0	0 0 0 0 1 1	−	0 0 0 1	−
F/F test	TTM			Test and reset timer F/F, then skip if it has not been set	if Timer F/F=1, then Timer F/F←0 if Timer F/F=0, then skip	1 0 1 0 0 1	−	−	−
	TUL			Test and reset unlock F/F, then skip if it has not been set	if UL F/F=1, then UL F/F←0 if UL F/F=0, then skip	1 0 1 0 1 0	−	−	−
	TKLT			Test then reset Key Latch F/F, then skip if true	if KL F/F=1, then skip and KL F/F←0	1 0 1 0 0 0	−	0 0 0 1	−
	TKLF			Test then reset Key Latch F/F, then skip if false	if KL F/F=1, then KL F/F←0 if KL F/F=0, then skip	1 0 1 0 0 0	0 1	0 0 0 1	−
Test timer	TIP			Test interval pulse, then skip if low	if IPG=0, then skip	1 0 1 0 0 1	−	0 0 0 0	0 0 0 0
IF counter	IFCW	w		Set immediate data to IFCW	IFCW←w	0 0 0 0 0 0	1 0	0 0 0 0	w
	IFC	t		Trigger and/or reset IF counter	Trigger←t_1, Reset←t_0	0 0 0 0 0 0	0 1	0 0 0 0	0 0 t
	TGC			Test IF counter gate, skip if close	if IFC gate=close, then skip	1 0 1 0 0 1	0 0	−	−

	Mnemonic	Operand 1ST	Operand 2ND	Function	Operation	Machine code: Operation code			
Status word and terminal test	SS	N_1		Set status word 1	(STATUS WORD 1)$_N$←1	000001	–	N_1	–
	RS	N_1		Reset status word 1	(STATUS WORD 1)$_N$←0	000011	–	N_1	–
	TST	N_2		Test status word 2 true	if (STATUS WORD 2)$_N$=all 1, then skip	001001	–	N_2	–
	TSF	N_2		Test status word 2 false	if (STATUS WORD 2)$_N$=all 0, then skip	001000	–	N_2	–
	STC			Set carry F/F	carry F/F←1	000001	–	0010	–
	RSC			Reset carry F/F	carry F/F←0	000011	–	0010	–
	BANK0			Select BANK0	BANK F/F0←0, BANK F/F1←0	000011	–	1100	–
	BANK1			Select BANK1	BANK F/F0←1, BANK F/F1←0	000001	–	0100	–
	BANK2			Select BANK2	BANK F/F0←0, BANK F/F1←1	000001	–	1000	–
	BANK3			Select BANK3	BANK F/F0←1, BANK F/F1←1	000001	–	1100	–
	TITT			Test INT, skip if true	if $\overline{INT}$=0, then skip	001001	–	0001	–
	TITF			Test INT, skip if false	if $\overline{INT}$=1, then skip	001000	–	0001	–
	TCET			Test CE, skip if true	if CE=1, then skip	001001	–	0010	–
	TCEF			Test CE, skip if false	if CE=0, then skip	001000	–	0010	–
	SBK0			Skip if BANK0	if BANK F/F0=BANK F/F1=0, then skip	001000	–	1100	–
	TB0T			Test BANK F/F0, skip if true	if BANK F/F0=1, then skip	001001	–	0100	–
	TB0F			Test BANK F/F0, skip if false	if BANK F/F0=0, then skip	001000	–	0100	–
	TB1T			Test BANK F/F1, skip if true	if BANK F/F1=1, then skip	001001	–	1000	–
	TB1F			Test BANK F/F1, skip if false	if BANK F/F1=0, then skip	001000	–	1000	–
Input / output	LCDD	M	D	Output segment pattern to LCD digit 'D' based on memory, or output to LCD digit directly	LCD(D)←SEG PLA←(M), or LCD(D)←(M)	100111	D_H	D	D_L
	KI	M		Input key data to memory	M←K_{e-1}	010000	D_H	D_L	0000
	KIN	M		Input key data to memory, then skip if data are zero	M←K_{e-1}, skip if(M)=0	010000	D_H	D_L	–
	IN	r	P	Input data on port to register	r←(Port (P))	110010	P	–	Rn
	OUT	P	r	Output contents of register to port	(Port (P))←(r)	100010	P	–	Rn
	SPB	P	N	Set port bits	(Port (P))$_N$←1	000001	P	0000	N
	RPB	P	N	Reset port bits	(Port (P))$_N$←0	000011	P	0000	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P))$_N$=all 1s, then skip	001001	P	0000	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P))$_N$=all 0s, then skip	001000	P	0000	N
Sirial I/O	SIO	s		Serial input/output	SMR (3,1,0)←s (3,1,0)	000000	00	0001	s
	TSET			Test shift end, then skip if true	if SCC=$\overline{s}$/(2n+1), then skip (n≥0)	101000	10	0001	–
	TSEF			Test shift end, then skip if false	if SCC=s/(2n+1), then skip (n≥0)	101000	00	0001	–
Test A/D	TADT			Test A–D comparator, then skip if true	if Vin > Vcomp, then skip	101000	00	0000	–
	TADF			Test A–D comparator, then skip if false	if Vin ≦ Vcomp, then skip	101000	10	0000	–
Others	CKSTP			Clock stop by CE	stop clock if CE=0	100011	–	1110	1110
	HALT	h		Halt the CPU. Restart by condition h	Halt	100011	00	–	h
	NOP			No operation		000000	–	–	–

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