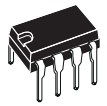
L6562AT

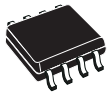
Transition-mode PFC controller

Features

- Guaranteed for extreme temperature range (outdoor)
- Proprietary multiplier design for minimum THD
- Very accurate adjustable output overvoltage protection
- Ultra-low (30 µA) start-up current
- Low (2.5 mA) quiescent current
- Digital leading-edge blanking on current sense
- Disable function on E/A input
- 1% (@ T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO and voltage clamp



DIP-8



SO-8

- DIP-8/SO-8 packages

Applications

PFC pre-regulators for:

- Street lighting
- IEC61000-3-2 compliant SMPS (Flat TV, monitors, desktop PC, games)
- Electronic ballast

Figure 1. Block diagram

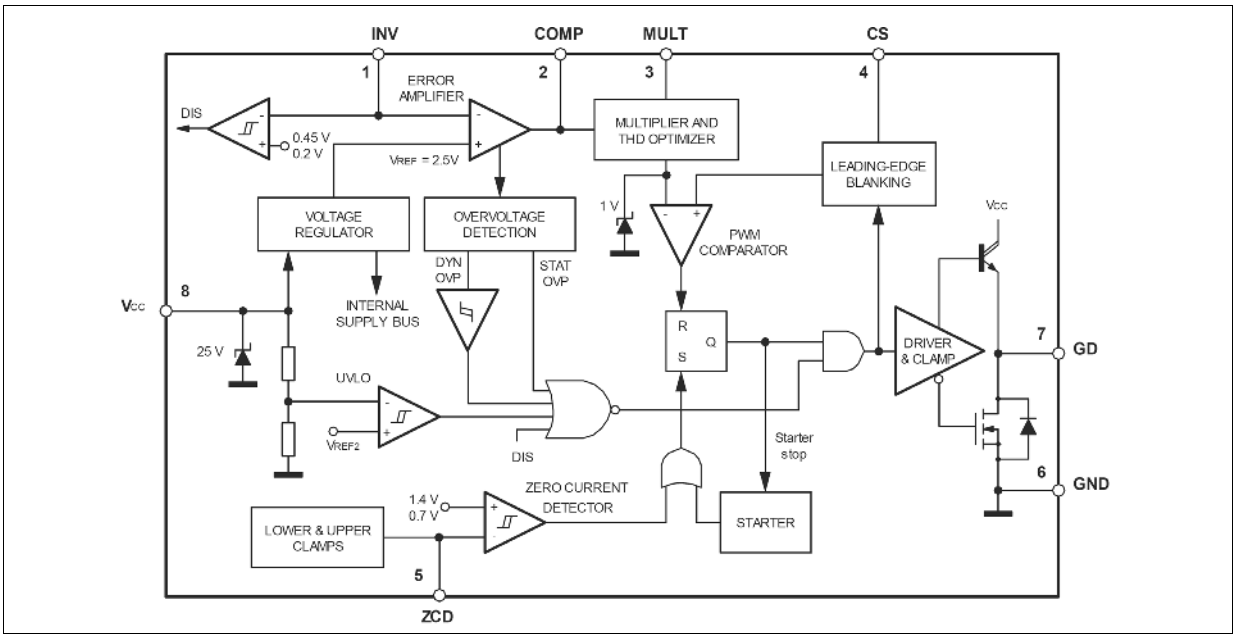


Table 1. Device summary

Order codes	Package	Packaging
L6562ATN	DIP-8	Tube
L6562ATD	SO-8	Tube
L6562ATDTR		Tape and reel

1 Description

The L6562AT is a current-mode PFC controller operating in transition mode (TM). Coming with the same pin-out as its predecessors L6561 and L6562, it offers improved performance.

The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @T_J = 25 °C) internal voltage reference.

The device features extremely low consumption (60 µA max. before start-up and < 5.5 mA operating) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving requirements (Blue Angel, EnergyStar, Energy2000, etc.).

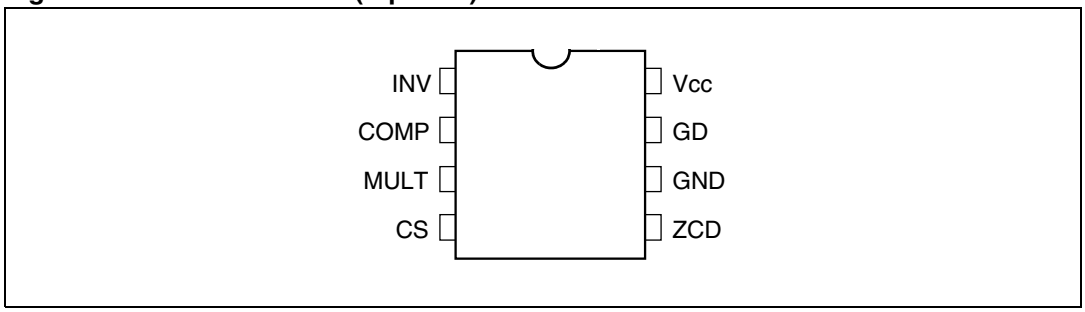
An effective two-step OVP enables to safely handle over-voltages either occurring at start-up or resulting from load disconnection.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable to drive high current MOSFETs or IGBTs. This, combined with the other features and the possibility to operate with the proprietary fixed-off-time control, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS in excess of 350 W.

2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 2. Pin description

Pin N°	Name	Description
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into this pin through a resistor divider. The pin doubles as an ON/OFF control input.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off. The pin is equipped with 200 ns leading-edge blanking for improved noise immunity.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22 V min. to provide more headroom for supply voltage changes.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	IC supply voltage ($I_{CC} \leq 20$ mA)	Self-limited	V
I_{GD}	7	Output totem pole peak current	Self-limited	A
---	1 to 4	Analog inputs and outputs	-0.3 to 8	V
I_{ZCD}	5	Zero current detector max. current	±10	mA

4 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		SO8	DIP8	
R_{thJA}	Max. thermal resistance, junction-to-ambient	150	100	°C/W
P_{TOT}	Power dissipation @T_A = 50 °C	0.65	1	W
T_J	Junction temperature operating range	-40 to 150		°C
T_{STG}	Storage temperature	-55 to 150		°C

5 Electrical characteristics

-40 °C < T_J < +125 °C, V_{CC} = 12 V, C_O = 1 nF; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	10.5		22.5	V
Vcc_{On}	Turn-on threshold	(1)	11.7	12.5	13.3	V
Vcc_{Off}	Turn-off threshold	(1)	9.5	10	10.5	V
Hys	Hysteresis		2.2		2.8	V
V_Z	Zener voltage	I_{CC} = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, V_{CC} = 11 V		30	60	µA
I_q	Quiescent current	After turn-on		2.5	3.9	mA
I_{CC}	Operating supply current	@ 70 kHz		3.5	5.5	mA
I_q	Quiescent current	During OVP (either static or dynamic) or $V_{INV} \leq$ 150 mV		1.7	2.2	mA
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 4 V			-1	µA
V_{MULT}	Linear operation range		0 to 3			V
$\frac{\Delta V_{cs}}{\Delta V_{MULT}}$	Output max. slope	V_{MULT} = 0 to 1 V, V_{COMP} = Upper clamp	1	1.1		V/V
K	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V,	0.32	0.38	0.47	V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.475	2.5	2.525	V
		10.5 V < V_{CC} < 22.5 V (1)	2.44		2.545	
	Line regulation	V_{CC} = 10.5 V to 22.5 V		2	5	mV
I_{INV}	Input bias current	V_{INV} = 0 to 3 V			-1	µA
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.1	5.7	6	V
	Lower clamp voltage	I_{SINK} = 0.5 mA (1)	2.1	2.25	2.4	V
V_{INVdis}	Disable threshold		150	200	250	mV
V_{INVen}	Restart threshold		380	450	520	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Output overvoltage						
I_{OVP}	Dynamic OVP triggering current		19.5	27	30.5	µA
Hys	Hysteresis	(3)		20		µA
	Static OVP threshold	(1)	2.1	2.25	2.4	V
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			-1	µA
t_{LEB}	Leading edge blanking		100	200	300	ns
$td_{(H-L)}$	Delay to output			175		ns
V_{CS}	Current sense clamp	V_{COMP} = Upper clamp, Vmult = 1.5 V	1.0	1.08	1.16	V
Vcs_{offset}	Current sense offset	V_{MULT} = 0		25		mV
		V_{MULT} = 2.5 V		5		
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7	6.5	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.5	0	0.5	V
V_{ZCDA}	Arming voltage (positive-going edge)	(3)		1.4		V
V_{ZCDT}	Triggering voltage (negative-going edge)	(3)		0.7		V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V		2		µA
I_{ZCDsrc}	Source current capability		-1.5			mA
I_{ZCDsnk}	Sink current capability		1.5			mA
Starter						
t_{START}	Start timer period		75	190	300	µs
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA		0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.5	10.3		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A
t_f	Voltage fall time			30	70	ns
t_r	Voltage rise time			60	130	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc = 0 to V_{CCon}, I_{sink} = 2 mA			1.1	V

1. All the parameters are in tracking
2. The multiplier output is given by: $V_{cs} = K \cdot V_{MULT} \cdot (V_{COMP} - 2.5)$
3. Parameters guaranteed by design, functionality tested in production.