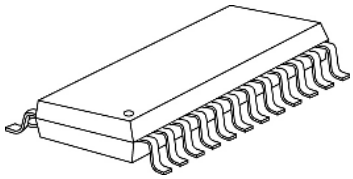
16-Channel PWM-Embedded LED Driver

Features

- Backward compatible with MBI5026 in package
- 16 constant-current output channels
- 16-bit/12-bit grayscale PWM control
- Scrambled-PWM technology to improve refresh rate
- Open-Circuit Detection to detect individual LED errors
- 8-bit programmable output current gain
- Over temperature warning
- Constant output current range:
  5 ~ 45mA at 3.3V supply voltage
  5 ~ 60mA at 5.0V supply voltage
- Output current accuracy:
  between channels: <±3% (max.), and
  between ICs: <±6% (max.)
- Staggered output delay
- Maximum data clock frequency: 25MHz
- Schmitt trigger input
- 3.0V-5.5V supply voltage

Small Outline Package



GF: SOP24-300-1.00

Product Description

MBI5030 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16-bit or 12-bit gray scales. MBI5030 features a 16-bit shift register which converts serial input data into each pixel gray scale of output port. At MBI5030 output port, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of Vf variations. The output current can be preset through an external resistor. Moreover, the preset current of MBI5030 can be further programmed up or down to 128 gain steps for LED global brightness adjustment.

With Scrambled-PWM (S-PWM™) technology, MBI5030 enhances Pulse Width Modulation by scrambling the “on” time into several “on” periods. The enhancement equivalently increases the visual refresh rate. When building a 16-bit gray scale video, S-PWM™ reduces the flickers and improves the fidelity. MBI5030 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5030 drives the corresponding LEDs to the brightness specified by image data. With MBI5030, all output channels can be built with 16-bit color depths (65,536 gray scales). Each LED’s brightness can be calibrated enough from minimum to maximum brightness with compensated gamma correction or LED deviation information inside the 16-bit image data.

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Block Diagram

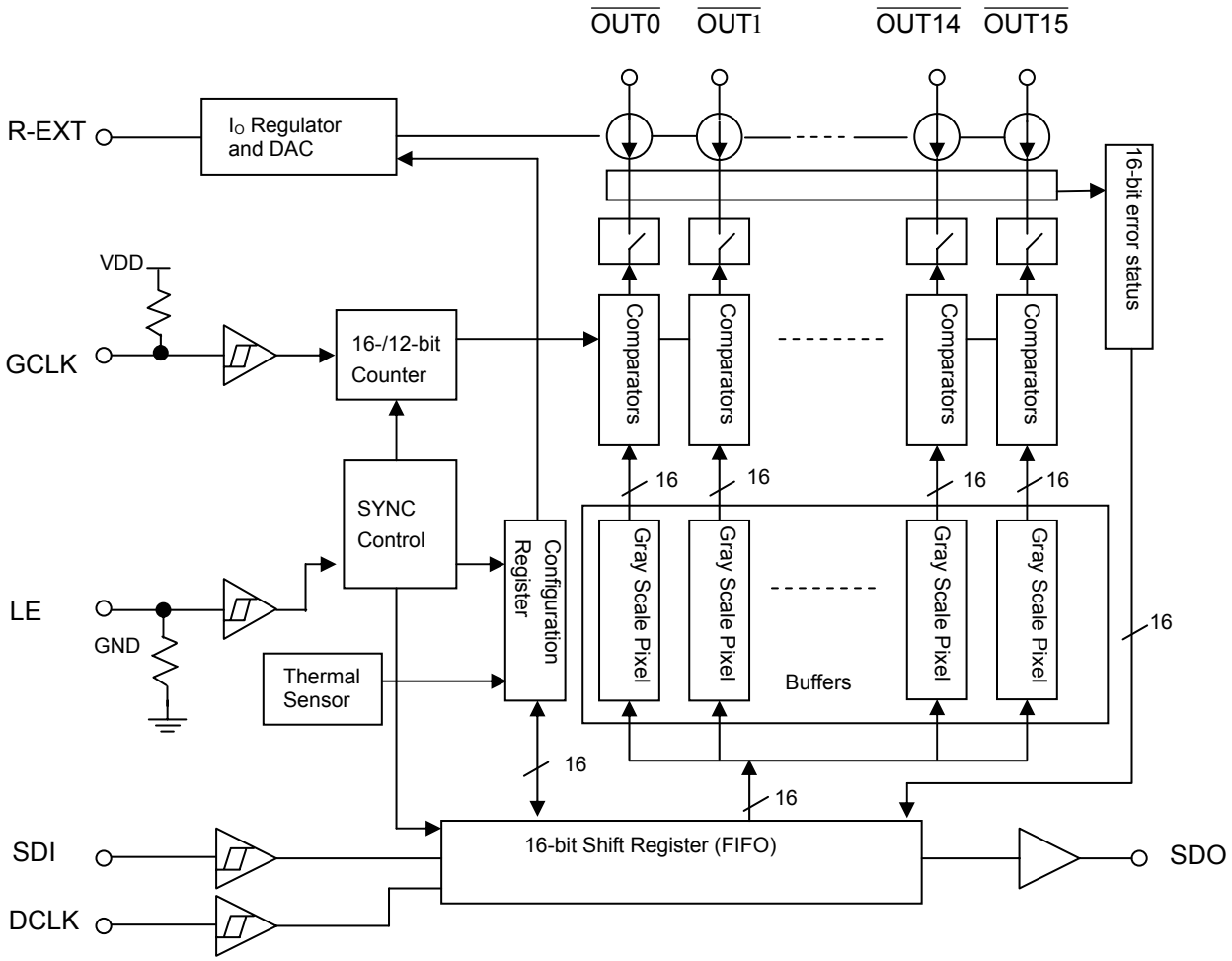
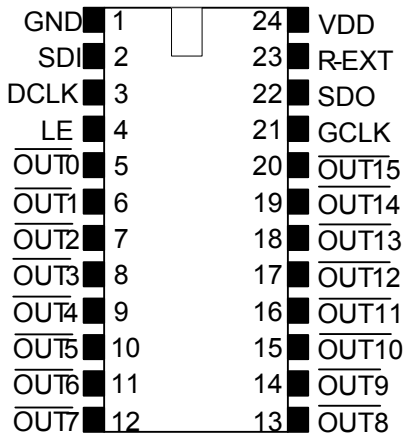


Figure 1

Terminal Description

Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Pin Configuration



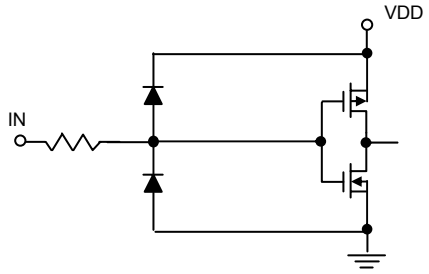
Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	7	V
Input Pin Voltage (SDI)		V_{IN}	-0.4 ~ V_{DD} + 0.4	V
Output Current		I_{OUT}	+60	mA
Sustaining Voltage at OUT Port		V_{DS}	17	V
Data Clock Frequency*		F_{DCLK}	+25	MHz
Gray Scale Clock Frequency		F_{GCLK}	+8	MHz
GND Terminal Current		I_{GND}	+1000	mA
Power Dissipation (On PCB, Ta=25°C)	GF Type	P_D	2.39	W
Thermal Resistance (On PCB, Ta=25°C)	GF Type	$R_{th(j-a)}$	52.37	°C/W
Operating Temperature		T_{opr}	-40 ~ +85	°C
Storage Temperature		T_{stg}	-55 ~ +150	°C

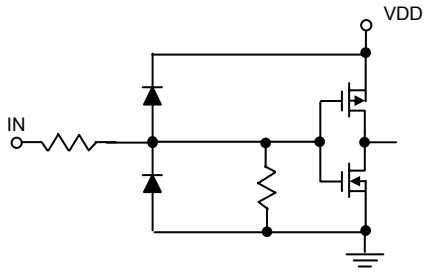
* Supply Voltage is 5V.

Equivalent Circuits of Inputs and Outputs

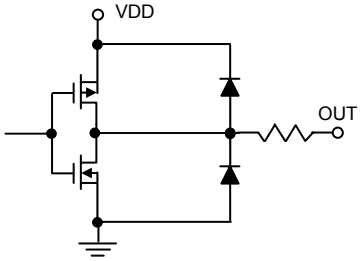
GCLK, DCLK, SDI terminal



LE terminal



SDO terminal



Electrical Characteristics (V_{DD}= 5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"	5	-	60	mA
		I_{OH}	SDO	-	-	-1.0	mA
		I_{OL}	SDO	-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC	0.7*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC	GND	-	0.3*V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}= 17.0V	-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}= +1.0mA	-	-	0.4	V
		V_{OH}	I_{OH}= -1.0mA	4.6	-	-	V
Current Skew		dI_{OUT}	I_{OUT}= 10.5mA, V_{DS}= 1.0V, R_{ext}= 920Ω	-	-	±3	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=460Ω@21mA	-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V, R_{ext}=460Ω@21mA	-	±1.0	-	% / V
LED Open Detection Threshold		$V_{DS,TH}$	-	-	0.15	0.20	V
Pull-down Resistor		R_{IN}(down)	LE	250	370	500	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}= Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off	-	3.5	5.3	mA
		I_{DD}(off) 2	R_{ext}= 920Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off	-	7.1	10.7	
		I_{DD}(off) 3	R_{ext}= 460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off	-	7.5	11.3	
	"On"	I_{DD}(on) 1	R_{ext}= 920Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = On	-	11.0	16.5	
		I_{DD}(on) 2	R_{ext}= 460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = On	-	11.5	17.3	
Thermal Flag Temperature		T_{TF}	Junction Temperature	135	150	165	°C

Electrical Characteristics (V_{DD}= 3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		5	-	45	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC		0.7*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC		GND	-	0.3*V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}= 17.0V		-	-	0.5	µA
Output Voltage	SDO	V_{OL}	I_{OL}= +1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}= -1.0mA		2.9	-	-	V
Current Skew		dI_{OUT}	I_{OUT}= 10.5mA V_{DS}= 1.0V	R_{ext}= 920Ω	-	-	±3	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=460Ω@21mA		-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V and 3.6V, R_{ext}=460Ω@21mA		-	±1.0	-	% / V
LED Open Detection Threshold		$V_{DS,TH}$	-		-	0.15	0.20	V
Pull-down Resistor		R_{IN}(down)	LE		250	370	500	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}= Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off		-	2.2	3.3	mA
		I_{DD}(off) 2	R_{ext}= 920Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off		-	4.4	6.6	
		I_{DD}(off) 3	R_{ext}= 460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off		-	6.3	9.5	
	"On"	I_{DD}(on) 1	R_{ext}= 920Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = On		-	6.7	10.1	
		I_{DD}(on) 2	R_{ext}= 460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ = On		-	7.1	10.7	
Thermal Flag Temperature		T_{TF}	Junction Temperature		135	150	165	°C

Test Circuit for Electrical Characteristics

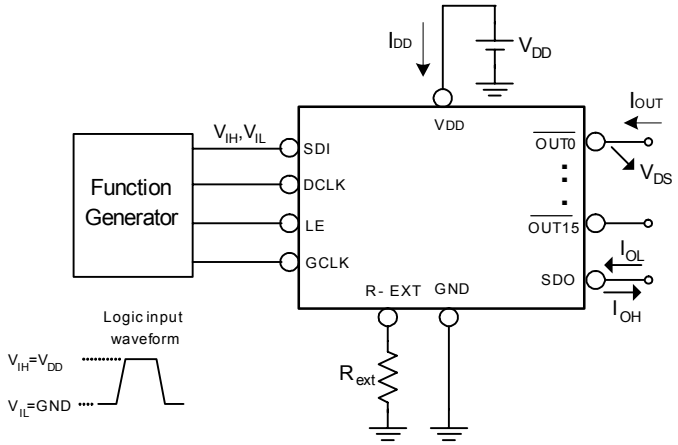


Figure 2

Switching Characteristics (V_{DD}= 5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=460Ω V_{LED}=4.5V R_L=152Ω C_L=10pF C_1=100nF C_2=10 μF	1	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		1	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		5	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		3	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7.0	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		15.0	22.0	35.0	ns
	GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	130	-	ns
	LE – SDO**	t_{PD2}**		16.0	24.0	37.0	ns
Stagger Delay Time	$\overline{OUT4n+1}$*	t_{DL1}		-	30.0	-	ns
	$\overline{OUT4n+2}$*	t_{DL2}		-	60.0	-	ns
	$\overline{OUT4n+3}$*	t_{DL3}		-	90.0	-	ns
Pulse Width	LE	$t_{w(L)}$		5.0	-	-	ns
	DCLK	$t_{w(DCLK)}$		20.0	-	-	ns
	GCLK	$t_{w(GCLK)}$		125.0	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	90.0	-	ns
Output Fall Time of Output Ports		t_{OF}		-	70.0	-	ns
Error Detection Minimum Duration		t_{EDD}***		-	2.0	-	μs

*There will be one GCLK latency at the first PWM output data. Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Refer to Figure 6.

Switching Characteristics (V_{DD}= 3.3V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=460Ω V_{LED}=4.5V R_L=152Ω C_L=10pF C_1=100nF C_2=10 μF	1.0	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		1.0	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		5.0	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		3.0	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7.0	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	40.0	-	ns
	GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	150	-	ns
	LE – SDO	t_{PD2}**		-	40.0	-	ns
Stagger Delay Time	$\overline{OUT4n+1}$*	t_{DL1}		-	30.0	-	ns
	$\overline{OUT4n+2}$*	t_{DL2}		-	60.0	-	ns
	$\overline{OUT4n+3}$*	t_{DL3}		-	90.0	-	ns
Pulse Width	LE	$t_{w(L)}$		5.0	-	-	ns
	DCLK	$t_{w(DCLK)}$		25.0	-	-	ns
	GCLK	$t_{w(GCLK)}$		125.0	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	90.0	-	ns
Output Fall Time of Output Ports		t_{OF}		-	70.0	-	ns
Error Detection Minimum Duration		t_{EDD}***		-	2.0	-	μs

*There will be one GCLK latency at the first PWM output data. Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Refer to Figure 6.

Test Circuit for Switching Characteristics

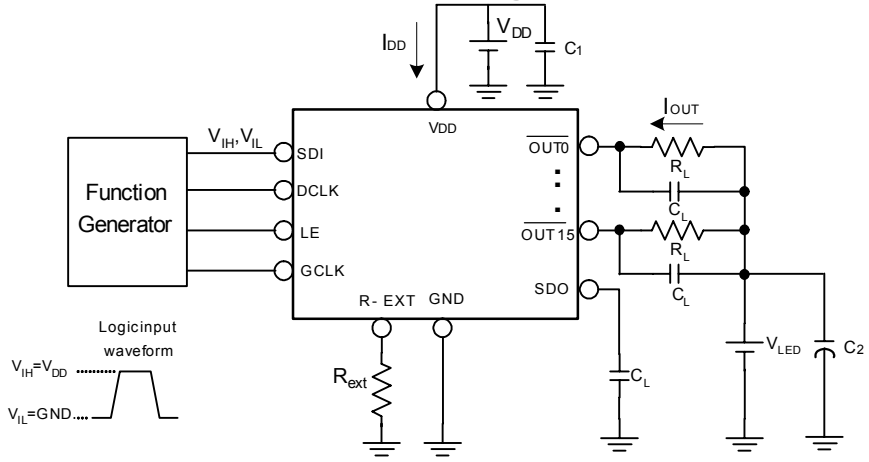
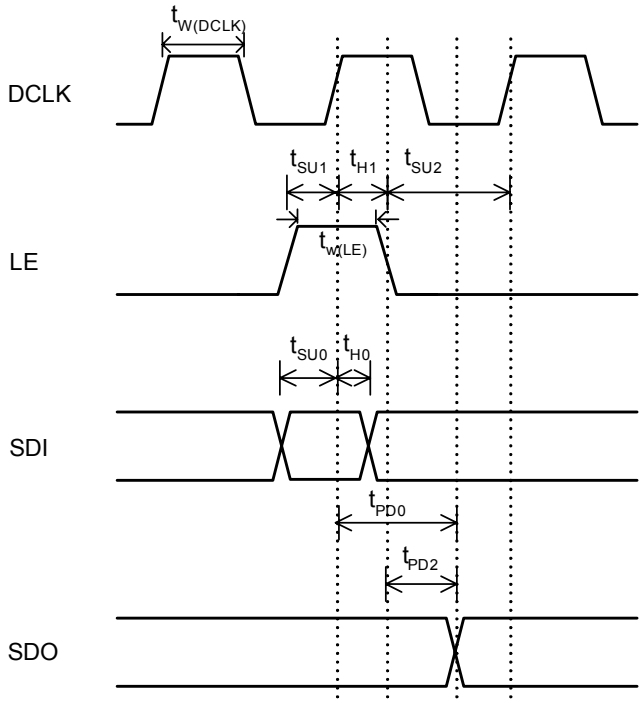


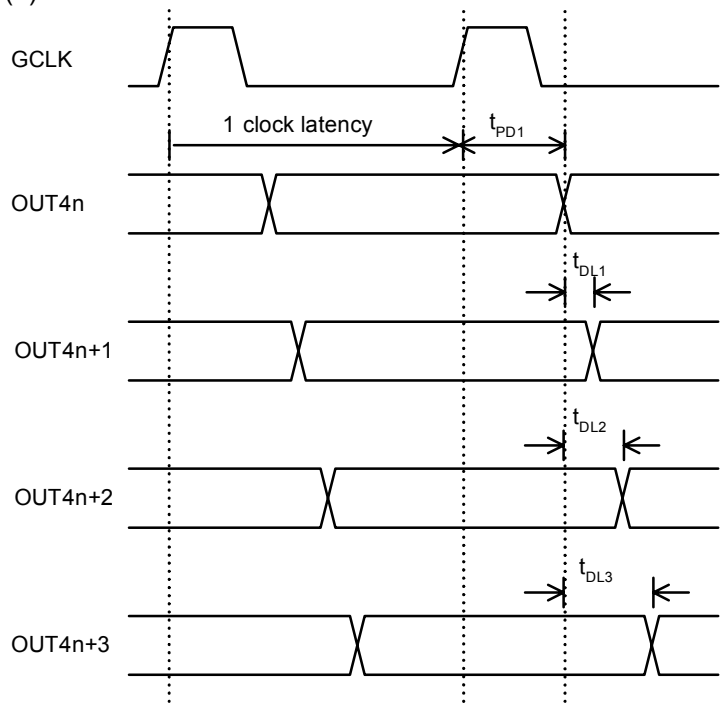
Figure 3

Timing Waveform

(1)



(2)



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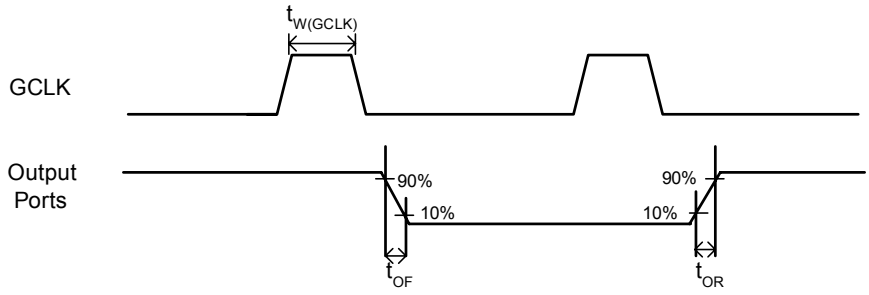
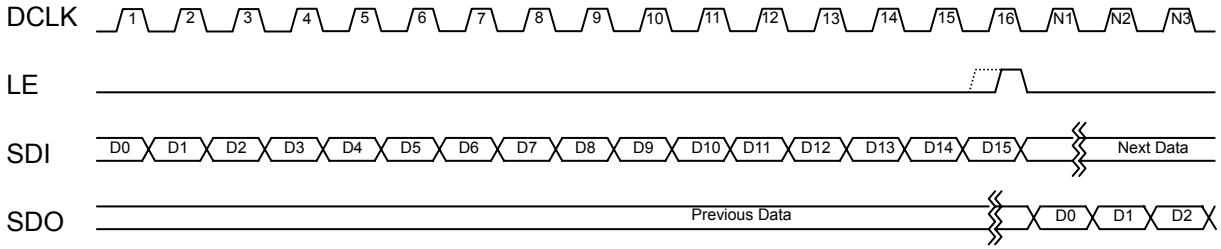


Principle of Operation

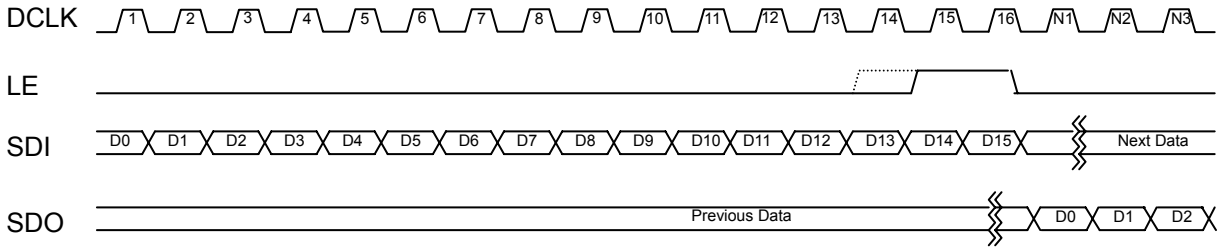
Control Command

	Signals Combination		Description
Command Name	**LE**	**Number of DCLK Rising Edge when LE is asserted**	**The Action after a Falling Edge of LE**
Data Latch	High	0 or 1	Serial data are transferred to the buffers
Global Latch	High	2 or 3	Buffer data are transferred to the comparators
Read Configuration	High	4 or 5	Move out “configuration register” to the shift registers
Enable “Error detection”	High	6 or 7	Enable “open circuit detection” of each output’s LED
Read “Error status code”	High	8 or 9	Move out “error status code” of 16 outputs to the shift registers
Write Configuration	High	10 or 11	Serial data are transferred to the “configuration register”

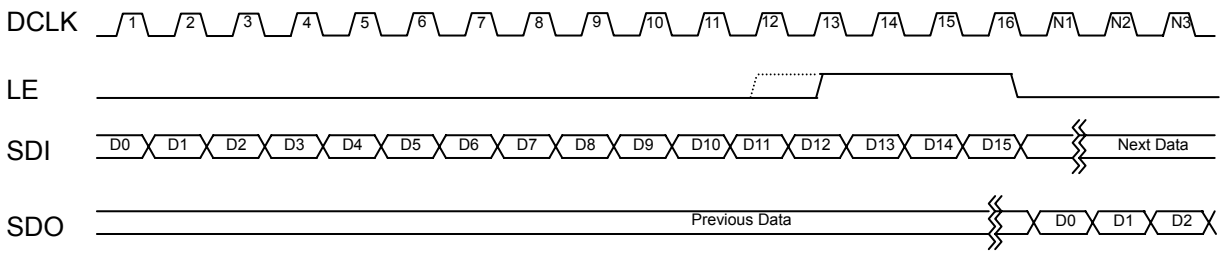
Data Latch



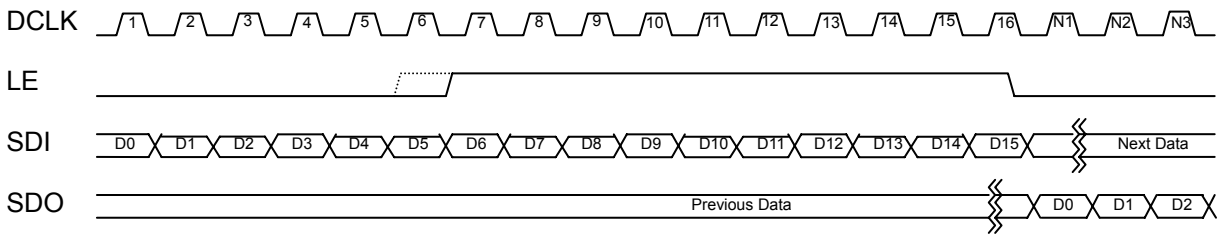
Global Latch



Read Configuration



Write Configuration



Setting Gray Scales of Pixels

MBI5030 implements the gray level of each output port using the S-PWM™ control algorithm. With the 16-bit data, all output channels can be built with 65,536 gray scales. The 16-bit input shift register latches 15 times of the gray scale data into each data buffer with a "data latch" command sequentially. With a "global latch" command for the 16th gray scale data, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.

Full Timing for Data Loading

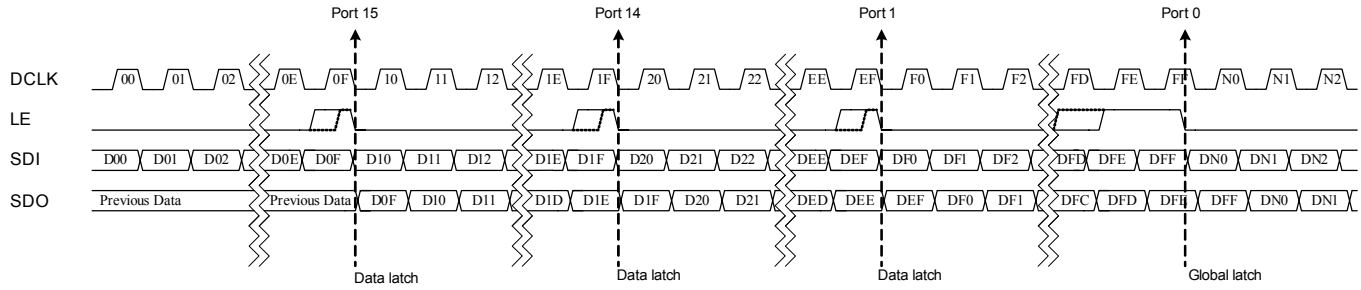


Figure 4

Open-Circuit Detection Principle

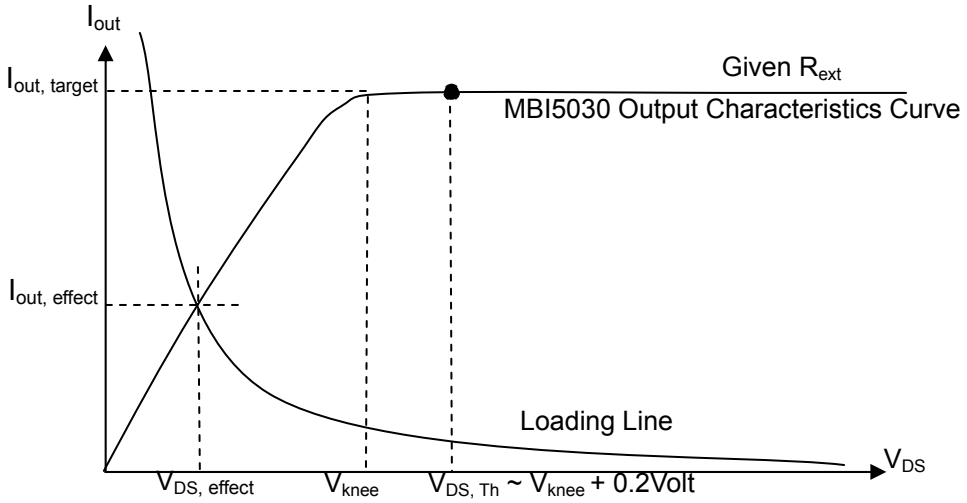
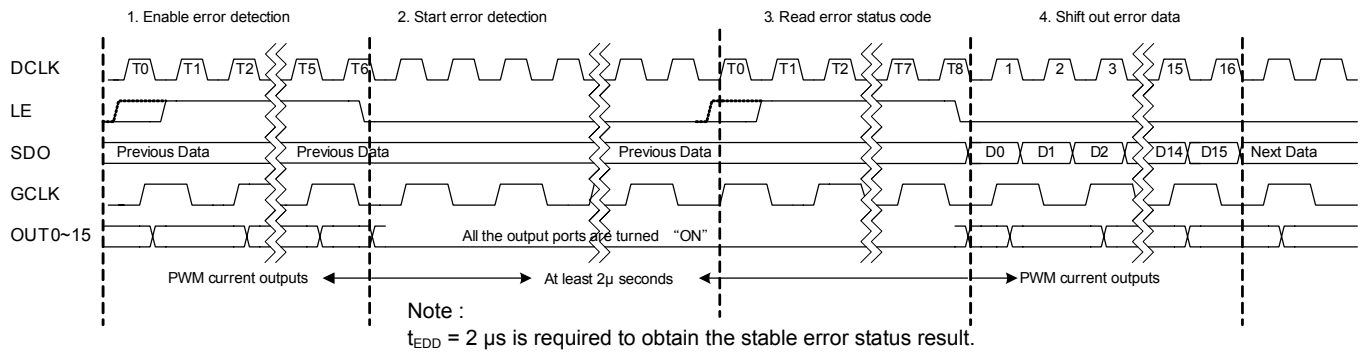


Figure 5

The principle of MBI5030 LED Open-Circuit Detection is based on the fact that the LED loading status is judged by comparing the effective current value ($I_{out, effect}$) of each output port with the target current ($I_{out, target}$) set by R_{ext}. As shown in the above figure, the knee voltage (V_{knee}) is the one between triode region and saturation region. The cross point between the loading line and MBI5030 output characteristics curve is the effective output point ($V_{DS, effect}$, $I_{out, effect}$).Thus, after the command of "enabling error detection", the output ports of MBI5030 will be turned on for a while. It is required to obtain the stable error status result for 2μ second. Then, the error status saved in the built-in register would be shifted out through SDO pin bit by bit by sending the command of "Read Error Status Code",

State of Output Port	Condition of Effective Output Point	Detected Open-Circuit Error Status Code	Meaning
Off	$I_{out, effect} = 0$	"0"	-
On	$I_{out, effect} \leqq I_{out, target}$ and $V_{out, effect} < V_{DS, Th}$	"1"	Open Circuit
	$I_{out, effect} = I_{out, target}$ and $V_{out, effect} \geqq V_{DS, Th}$	"0"	Normal
Note: the threshold voltage $V_{DS, Th}$ is around V_{knee} + 0.2 Volt			



Note :
t_{EDD} = 2 μs is required to obtain the stable error status result.

Figure 6

Definition of Configuration Register

Bit	Attribute	Definition	Value	Function	
F	Read/Write	Parity bit (Even) of configuration register	0 (Default)	Correct	
			1	Parity error	
E	Read	Thermal error flag	0 (Default)	Safe (OK)	
			1	Over heating (>165 ℃)	
D	Write	PWM gray scale counter	0 (Default)	16 bits	
			1	12 bits	
C	Write	PWM counting mode selection	00 (Default)	When bit D is set to "0", 64 times of 10-bit PWM counting and once of 6-bit PWM counting	When bit D is set to "1", 64 times of 6-bit PWM counting and once of PWM 6-bit counting
			01	When bit D is set to "0", 16 times of 10-bit PWM counting by 1/4 GCLK and once of 6-bit PWM counting	When bit D is set to "1", 16 times of 6-bit PWM counting by 1/4 GCLK and once of 6-bit PWM counting
B			10	When bit D is set to "0", 4 times of 10-bit PWM counting by 1/16 GCLK and once of 6-bit PWM counting	When bit D is set to "1", 4 times of 6-bit PWM counting by 1/16 GCLK and once of 6-bit PWM counting
			11	16-bit PWM counting	12-bit PWM counting
A	Write	PWM data synchronization mode	0	Auto-synchronization	
			1	Self-synchronization	
9~2	Write	Current gain adjustment	00000000 ~ 11111111	8'b10101011 (Default)	
1	X	X	X	Reserved bit	
0	Write	Time-out alert of GCLK disconnection	0	Enable	
			1 (Default)	Disable	

Checking Parity Bit

The data of configuration register could refer to the use of even parity bit to check that data has been transmitted accurately. As the transmitting device sends 16-bit configuration register, it counts the total number of fifteen bits. If the number is even, it sets the parity bit to 0; if the number is odd, it sets the parity bit to 1. In this way, configuration register has an even number of 16 bits. Inside MBI5030, the device checks the configuration register to make sure that it has an even number of 16 bits. If it finds an odd number of 16 bits, the device knows there was an error during transmission and modified the parity bit to “1”, otherwise, the parity bit is set to “0” for correct transmission.

Thermal Error Flag

The thermal error flag indicates an overheating condition. When IC’s junction temperature is over 165°C (typical), the bit “E” is set to “1”. The bit “E” can be read out through “Read Configuration” command.

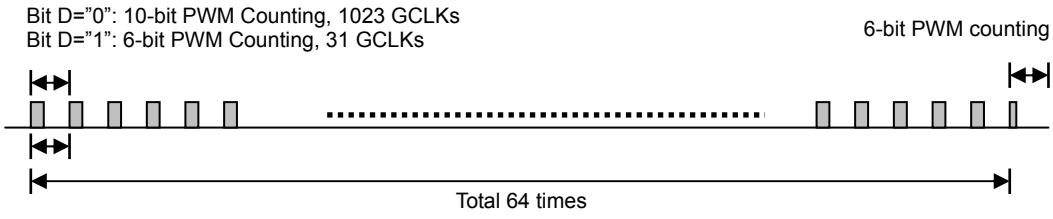
Setting the PWM Gray Scale Counter

MBI5030 provides a selectable 16-bit or 12-bit color depth. The value of 16-bit image pixel of each output will be only implemented according 16-bit or 12-bit PWM counter. The default bit “D” is set to “0” for 16-bit PWM gray scale.

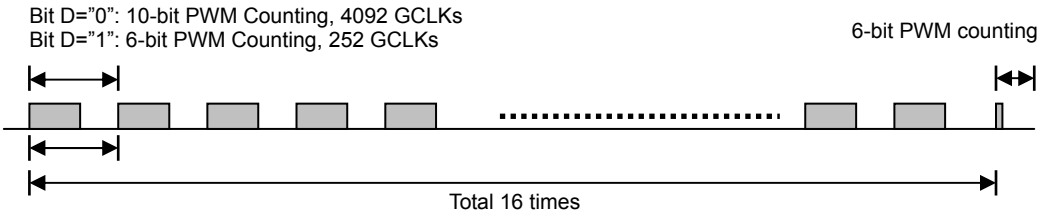
Setting the PWM Counting Mode

MBI5030 defines the different counting algorithms that support S-PWM™, scrambled PWM, technology. With S-PWM™ , the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution. MBI5030 also allows changing different counting algorithms and provides the better output linearity when there are fewer transitions of output.

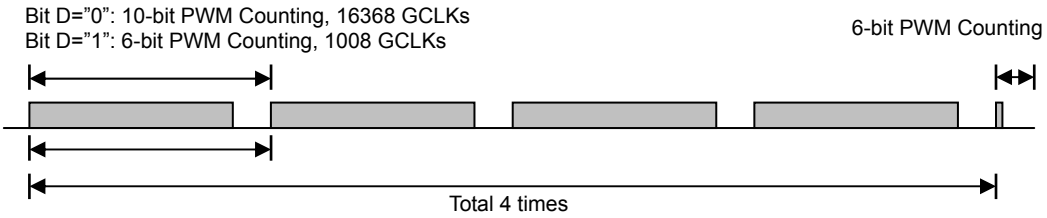
Mode 00
10-bit x 2^6 + 6-bit counting
# of GCLKs=$(2^{10}-1)x2^6+2^6$
6-bit x 2^6 + 6-bit counting
# of GCLKs=$(2^6-1)x2^6+2^6$



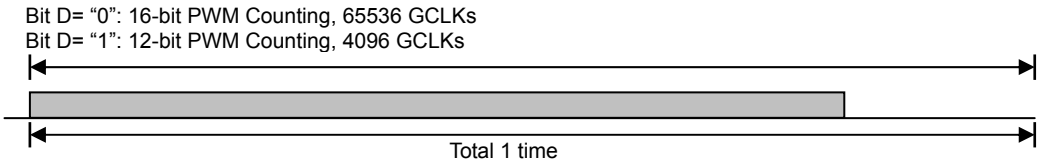
Mode 01
10-bit x 2^2x2^4 + 6-bit counting
# of GCLKs=$(2^{10}-1)x2^2x2^4+2^6$
6-bit x 2^2x2^4 + 6-bit counting
# of GCLKs=$(2^6-1)x2^2x2^4+2^6$



Mode 10
10-bit x 2^4x2^2 + 6-bit counting
# of GCLKs=$(2^{10}-1)x2^4x2^2+2^6$
6-bit x 2^4x2^2 + 6-bit counting
# of GCLKs=$(2^6-1)x2^4x2^2+2^6$



Mode 10
16 direct counting
# of GCLKs=2^{16}
12 direct counting
# of GCLKs=2^{12}



Synchronization for PWM Counting

Between the data frame and the video frame, when the bit “A” is set to “0” (Default), MBI5030 will automatically handle the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data has finished one internal PWM cycle. It will prevent the lost count of image data resolution and guarantee the data accuracy. In this mode, system controller only needs to provide a continuous running GCLK for PWM counter. The output will be renewed after finishing one of MSB PWM cycles.

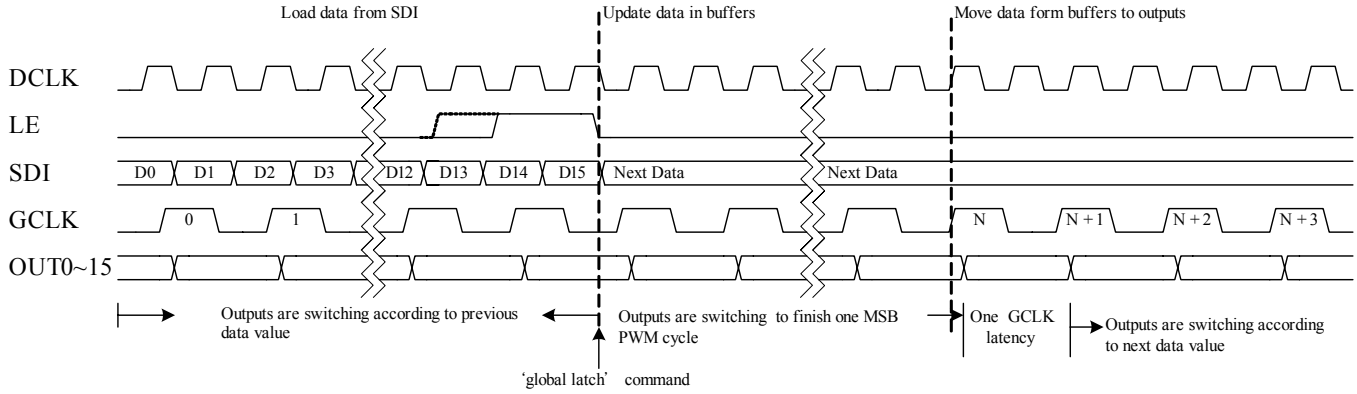


Figure 7

When the bit “A” is set to “1”, MBI5030 will update the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5030 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.

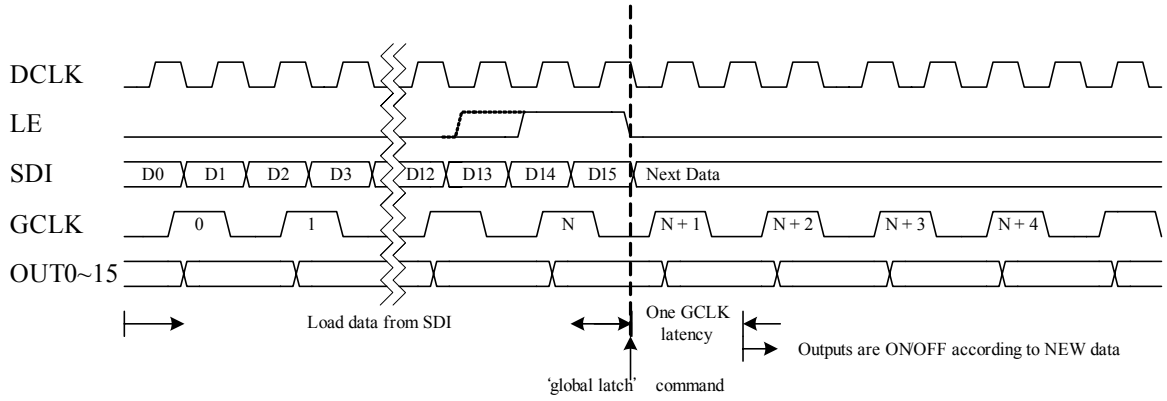


Figure 8

Time-Out Alert of GCLK Disconnection

When signal of GCLK is disconnected for around 1 second period, the all output ports will be turned off automatically. This function will protect the LED display system to stay on always and prevent a big current to damage the power system. The default is set to ‘disable” when bit “0” is 1. When the GCLK is active again, the driver resumes to work after resetting the internal counters and comparators.

Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

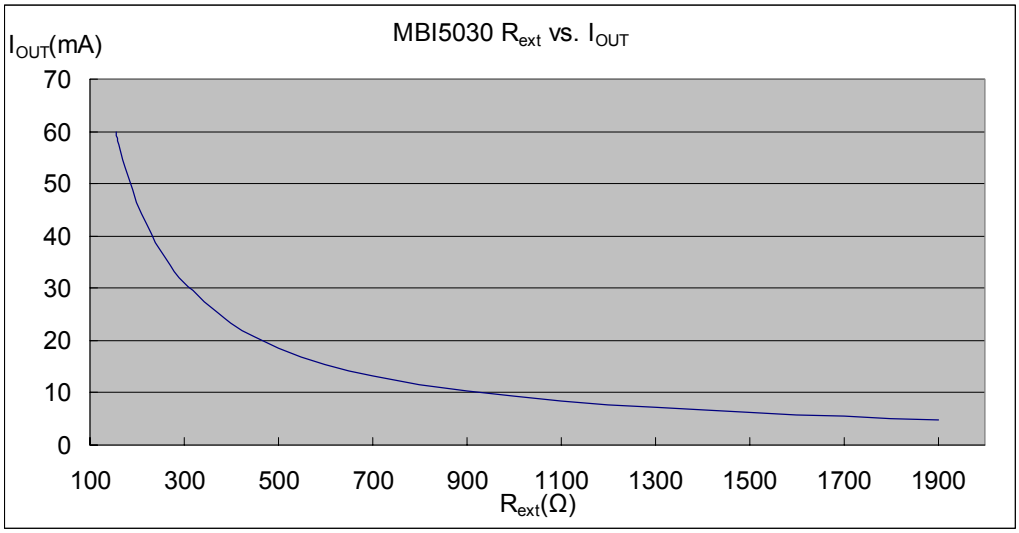


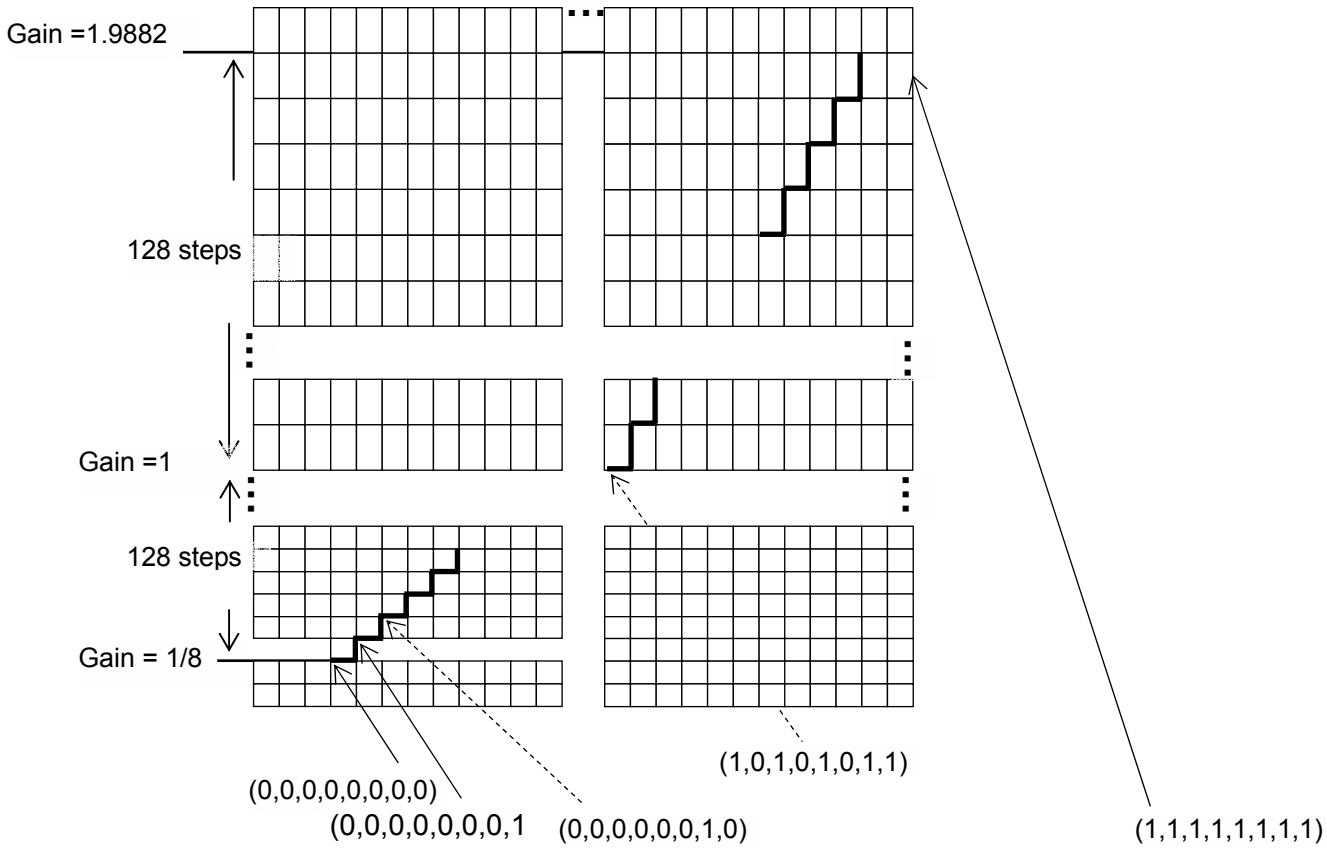
Figure 9

Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.625Volt x G; I_{OUT}= ($V_{R\text{-}EXT}$/R_{ext}) x15.5

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit9 – bit2 of the configuration register. The default value of G is 1. For your information, the output current is about 21mA when R_{ext}=460Ω and 10.5mA when R_{ext}=920Ω if G is set to default value 1. The formula and setting for G are described in next section.

- Current Gain Adjustment



The bit 9 to bit 2 of the configuration register set the gain of output current, i.e., G. As totally 8-bit in number, i.e., ranged from 8'b00000000 to 8'b11111111, these bits allow the user to set the output current gain up to 256 levels. These bits can be further defined inside Configuration Register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA6	DA5	DA4	DA3	DA2	DA1	DA0	-	-

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 2 are DA6 ~ DA0.

The relationship between these bits and current gain G is:

$G = [(1+3 \times HC)/4] \times [(1+3 \times D/128)/2]$

Whereas HC is 1 or 0 and

$D = DA6 \times 2^6 + DA5 \times 2^5 + DA4 \times 2^4 + DA3 \times 2^3 + DA2 \times 2^2 + DA1 \times 2^1 + DA0 \times 2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 7-bit mantissa DA6~DA0. For example,

1. When the bit9 to bit2 of configuration register are set to 8'b11111111, the current gain G becomes $[(1+3 \times 1)/4] \times [(1+3 \times 127/128)/2] = 1.9882$
2. When the bit9 to bit2 of configuration register are set to 8'b10000000, the current gain G becomes $[(1+3 \times 1)/4] \times [(1+3 \times 0/128)/2] = 0.5$
3. when the bit9 to bit2 of configuration register are set to 8'b00000000, the current gain G becomes $[(1+3 \times 0)/4] \times [(1+3 \times 0/128)/2] = 1/8$

Delay Time of Staggered Output

MBI5030 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 30ns delay time among $\overline{OUT4n}$, $\overline{OUT4n+1}$, $\overline{OUT4n+2}$, and $\overline{OUT4n+3}$, by which the output ports will be divided to four groups at a different time so that the instant current from the power line will be lowered.

Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as P_D (max) = (Tj – Ta) / $R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is P_D (act) = (I_{DD} x V_{DD}) + (I_{OUT} x Duty x V_{DS} x 16). Therefore, to keep P_D (act) ≤ P_D (max), the allowable maximum output current as a function of duty cycle is:

I_{OUT} = { [(Tj – Ta) / $R_{th(j-a)}$] – (I_{DD} x V_{DD}) } / V_{DS} / Duty / 16, where Tj = 150°C.

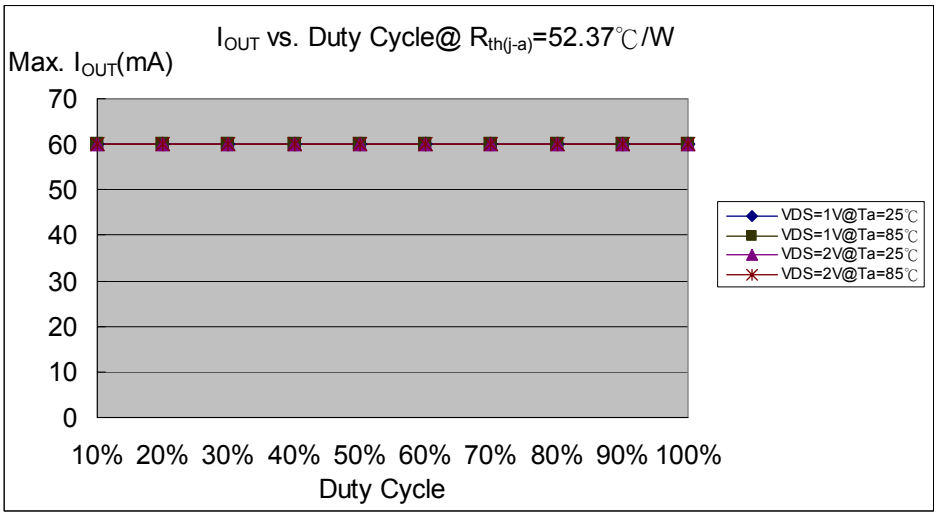


Figure 10

Condition: I_{OUT}=60mA, 16 output channels	
Device Type	$R_{th(j-a)}$ (°C /W)
GF	52.37

The maximum power dissipation, P_D (max) = (Tj – Ta) / $R_{th(j-a)}$, decreases as the ambient temperature increases.

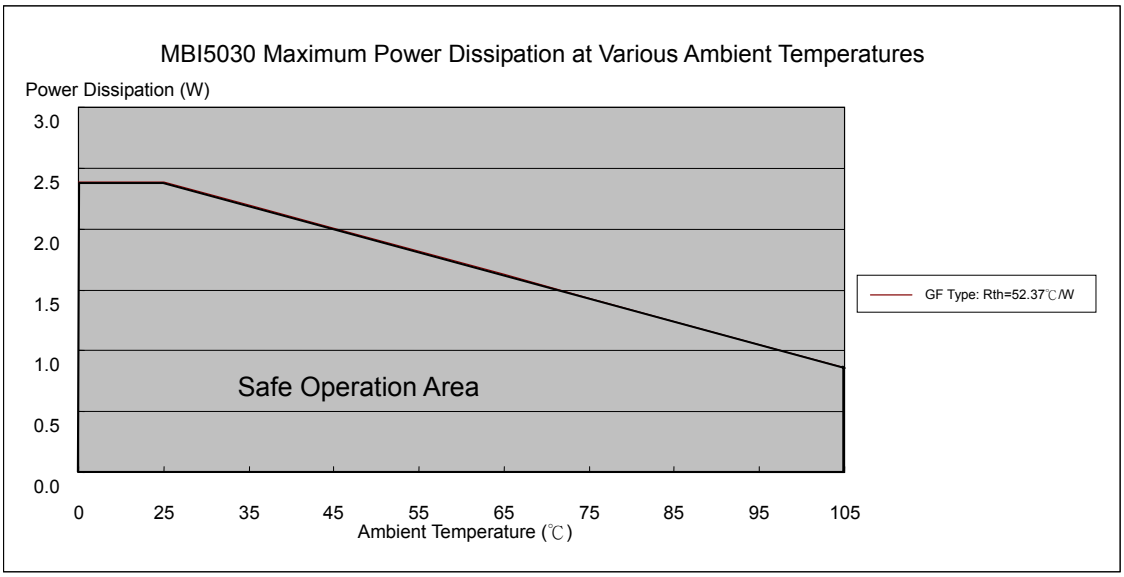


Figure 11

LED Supply Voltage (V_{LED})

MBI5030 are designed to operate with V_{DS} ranging from 0.4V to 0.8V (depending on I_{OUT}=5~60mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED} = 5V and V_{DS} = $V_{LED} – V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS} = (V_{LED} – V_F) – V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

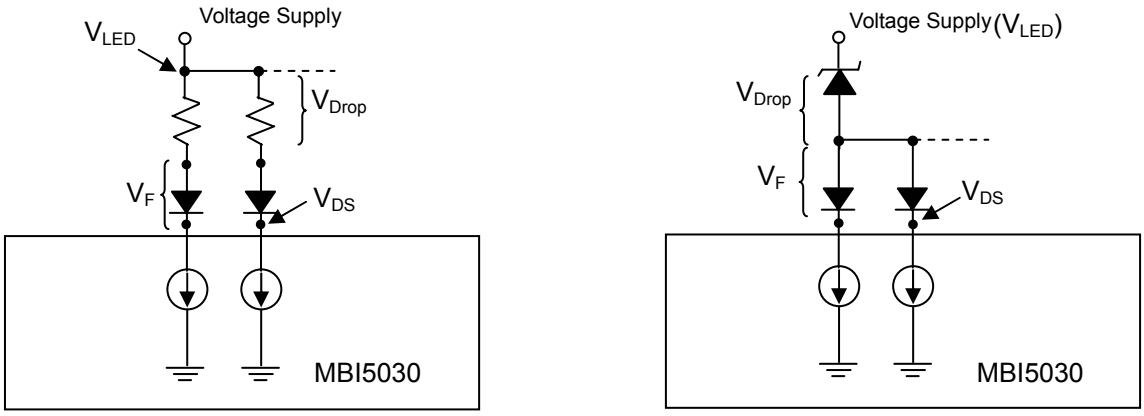
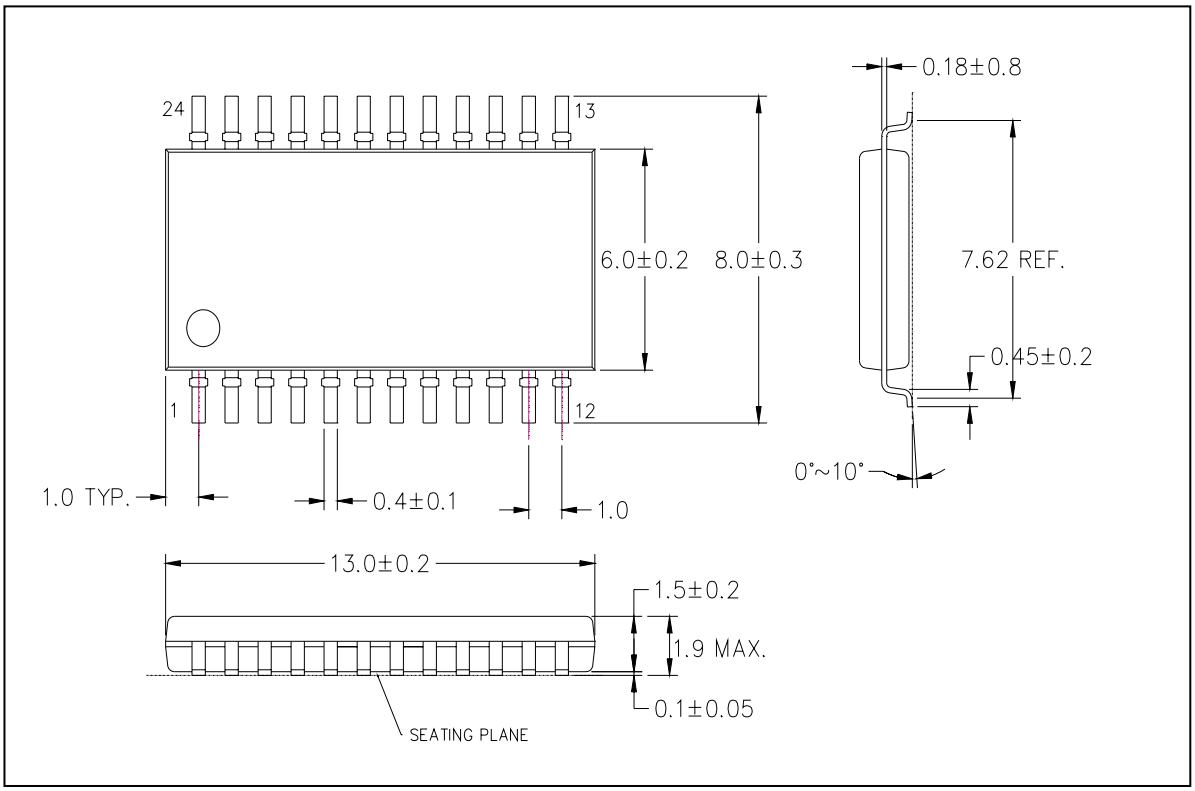


Figure 12

Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers-Overshoot”.

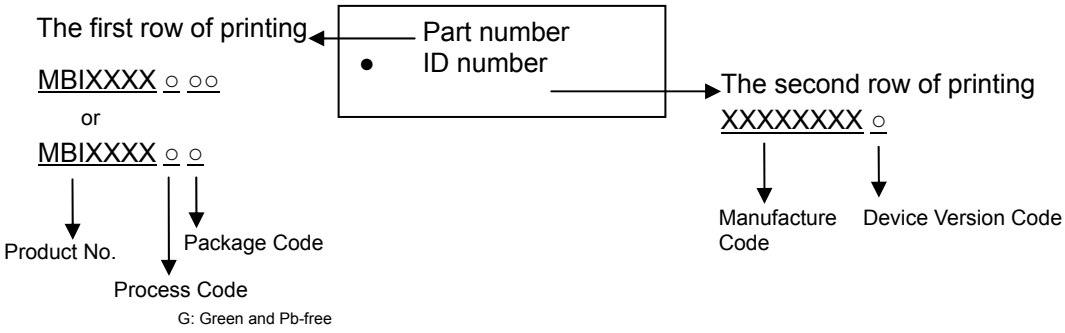
Package Outline



MBI5030GF Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top Mark Information



Product Revision History

Datasheet version	Device Version Code
V1.00	A

Product Ordering Information

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5030GF	SOP24-300-1.00	0.28