

8-Bit Serial or Parallel-Input/ Serial-Output Shift Register High-Performance Silicon-Gate CMOS

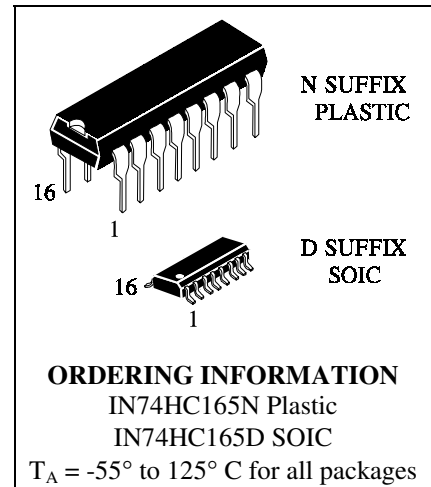
IN74HC165

The IN74HC165 is identical in pinout to the LS/ALS165. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

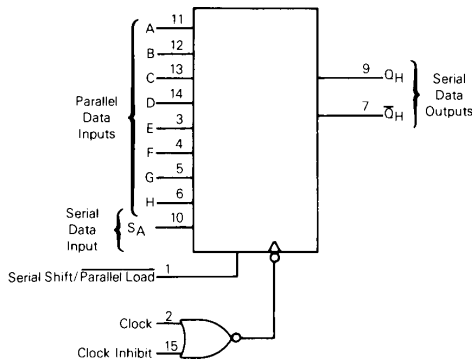
This device is an 8-bit shift register with complementary outputs from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Serial Shift/Parallel Load input is low, the data is loaded asynchronously in parallel. When the Serial Shift/Parallel Load input is high, the data is loaded serially on the rising edge of either Clock or Clock Inhibit (see the Function Table).

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT

Serial Shift/ Parallel Load	1 ●	16	V _{CC}
Clock	2	15	Clock Inhibit
E	3	14	D
F	4	13	C
G	5	12	B
H	6	11	A
\bar{Q}_H	7	10	S _A
GND	8	9	Q _H

FUNCTION TABLE

Inputs				Internal Stages		Output	Operation	
Serial Shift/ Parallel Load	Clock	Clock Inhibit	S _A	A-H	Q _A	Q _B -Q _G	Q _H	
L	H	X	X	a...h	a	b-g	h	Asynchronous Parallel Load
H		L	L	X	L	Q _{An} -Q _{Fn}	Q _{Gn}	Serial Shift via Clock
H		L	H	X	H	Q _{An} -Q _{Fn}	Q _{Gn}	
H	L		L	X	L	Q _{An} -Q _{Fn}	Q _{Gn}	Serial Shift via Clock Inhibit
H	L		H	X	H	Q _{An} -Q _{Fn}	Q _{Gn}	
H	X	H	X	X	no change			Inhibited Clock
H	H	X	X	X	no change			
H	L	L	X	X	no change			No Clock

X = Don't Care

Q_{An}-Q_{Fn} = Data shifted from the preceding stage

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	$^{\circ}C$

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$
SOIC Package: : - 7 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0\text{ V}$	0	1000	
	$V_{CC} = 4.5\text{ V}$	0	500	
	$V_{CC} = 6.0\text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48	5.34	5.2				
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} = V _{IL} or V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26	0.33	0.4				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	8.0	80	160	μA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock (or Clock Inhibit) to Q _H or Q _H (Figures 1 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay , SerialShift./Parallel Load to Q _H or Q _H (Figures 2 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input H to Q _H or Q _H (Figures 3 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Per Package)	Typical @25°C, V _{CC} =5.0 V			pF	
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	85				

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{SU}	Minimum Setup Time, Parallel Data Inputs to Serial Shift/Parallel Load (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{SU}	Minimum Setup Time, Input S _A to Clock (or Clock Inhibit) (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{SU}	Minimum Setup Time, Serial Shift/Parallel Load to Clock (or Clock Inhibit) (Figure 6)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{SU}	Minimum Setup Time, Clock to Clock Inhibit (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Serial Shift/Parallel Load to Parallel Data Inputs (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _h	Minimum Hold Time, Clock (or Clock Inhibit) to Input S _A (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _h	Minimum Hold Time, Clock (or Clock Inhibit) to Serial Shift/Parallel Load (Figure 6)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _{rec}	Minimum Recovery Time, Clock to Clock Inhibit (Figure 7)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _w	Minimum Pulse Width, Clock (or Clock Inhibit) (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

SWITCHING WAVEFORMS

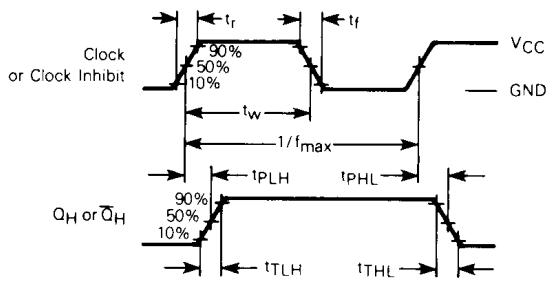


Figure 1. Serial-Shift Mode

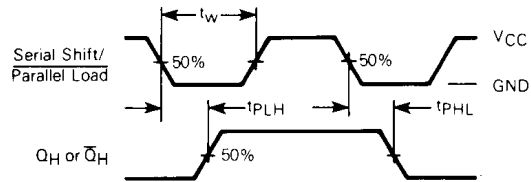


Figure 2. Parallel-Load Mode

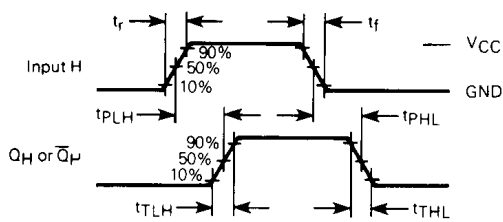


Figure 3. Parallel-Load Mode

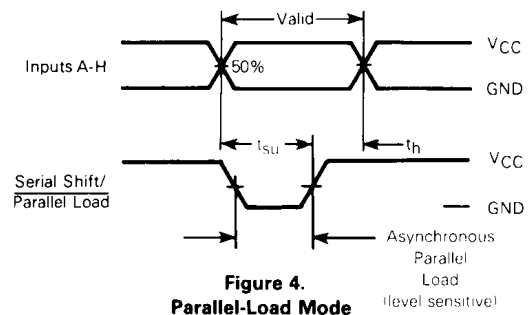


Figure 4. Parallel-Load Mode (level sensitive)

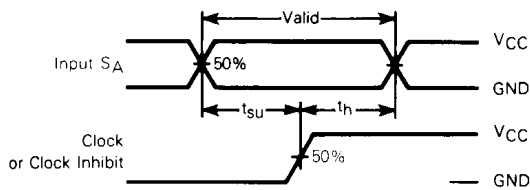


Figure 5. Serial-Shift Mode

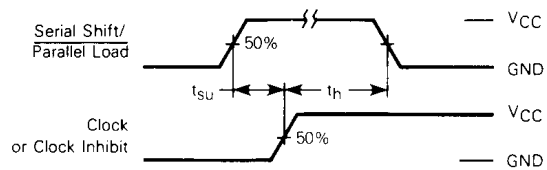


Figure 6. Serial-Shift Mode

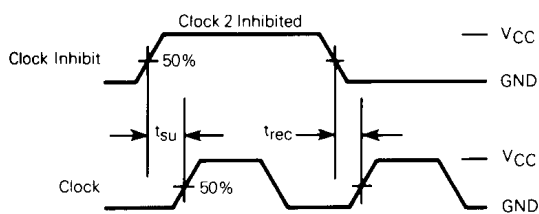
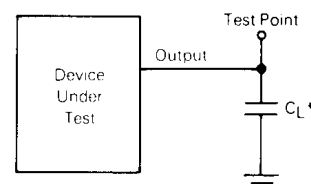


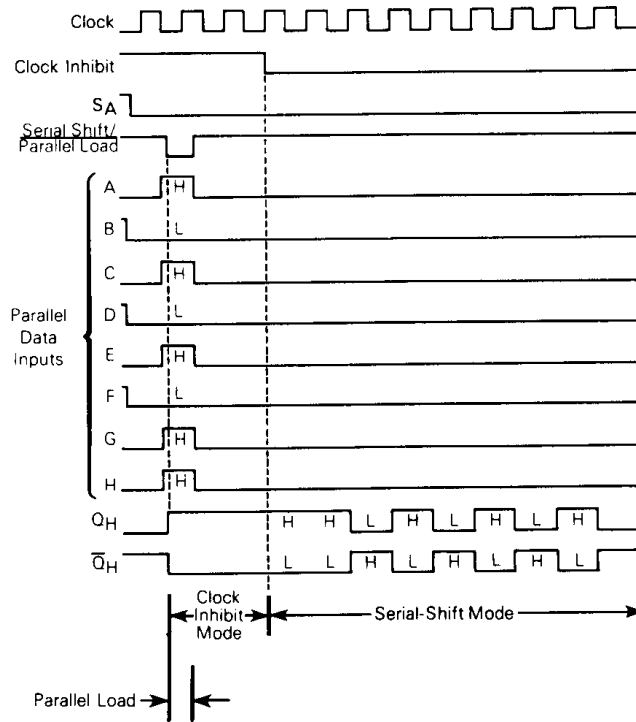
Figure 7. Serial-Shift, Clock-Inhibit Mode



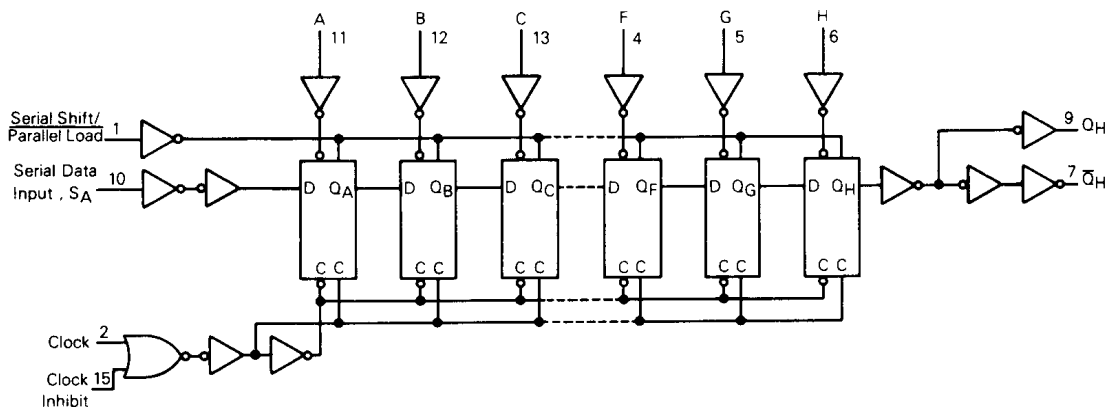
* Includes all probe and jig capacitance.

Figure 8. Test Circuit

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



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