

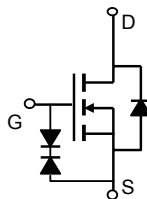
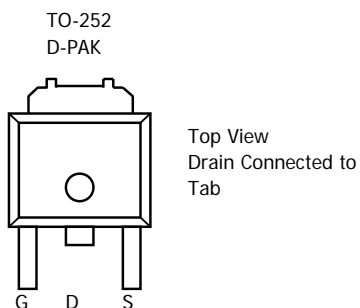
**AOD434**
**N-Channel Enhancement Mode Field Effect Transistor**

**General Description**

The AOD434 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 1.8V while retaining a 12V  $V_{GS(MAX)}$  rating. It is ESD protected to a 2KV HBM rating. *Standard Product AOD434 is Pb-free (meets ROHS & Sony 259 specifications). AOD434L is a Green Product ordering option. AOD434 and AOD434L are electrically identical.*

**Features**

$V_{DS}$  (V) = 20V  
 $I_D$  = 18A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)} < 14m\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)} < 16m\Omega$  ( $V_{GS}$  = 4.5V)  
 $R_{DS(ON)} < 21m\Omega$  ( $V_{GS}$  = 2.5V)  
 $R_{DS(ON)} < 30m\Omega$  ( $V_{GS}$  = 1.8V)  
 ESD Rating: 2KV HBM


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30	
Avalanche Current <sup>C</sup>	$I_{AR}$	18	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	37	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	16.7	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	40	50
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	1.9	2.5	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			10	μA
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	V <sub>DS</sub> =0V, I <sub>G</sub> =±250μA	±12			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	0.75	1	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =18A T <sub>J</sub> =125°C		10.9 14.3	14 18	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A		12.6	16	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =10A		16.5	21	mΩ
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =5A		23.2	30	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =18A		36		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.73	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				18	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =10V, f=1MHz		1810		pF
C <sub>oss</sub>	Output Capacitance			232		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			200		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		1.6		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V, I <sub>D</sub> =18A		40.1		nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			8.9		
Q <sub>gs</sub>	Gate Source Charge			1.7		nC
Q <sub>gd</sub>	Gate Drain Charge			6.2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V, R <sub>L</sub> =0.56Ω, R <sub>GEN</sub> =3Ω		4		ns
t <sub>r</sub>	Turn-On Rise Time			15		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			42.2		ns
t <sub>f</sub>	Turn-Off Fall Time			18.2		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =18A, dI/dt=100A/μs		23.2		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =18A, dI/dt=100A/μs		4.9		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

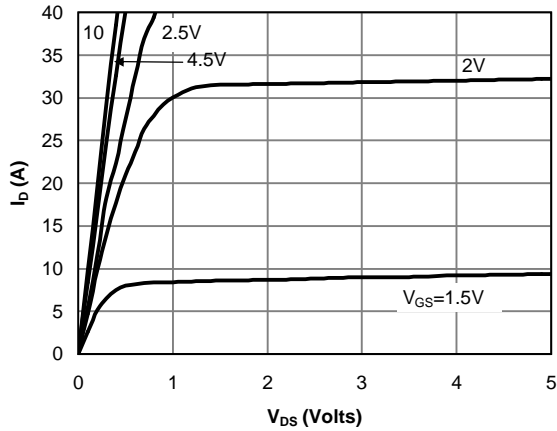


Fig 1: On-Region Characteristics

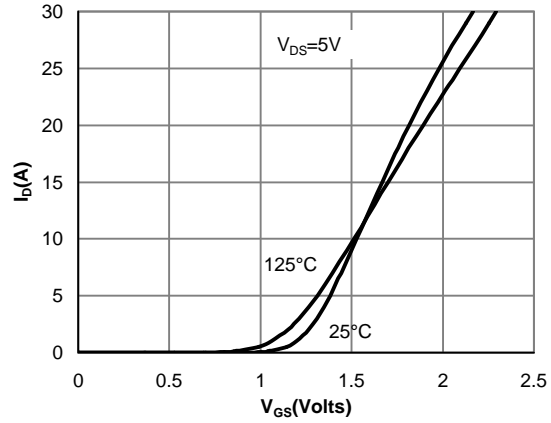


Figure 2: Transfer Characteristics

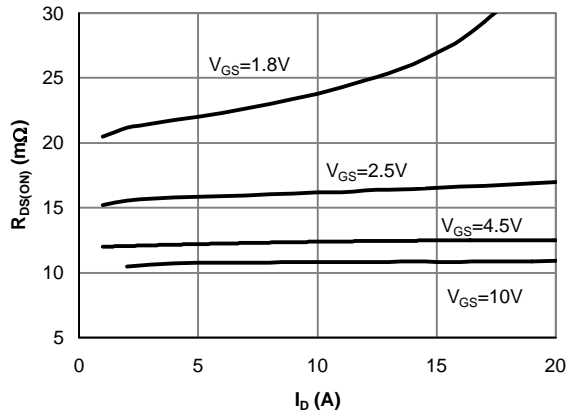


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

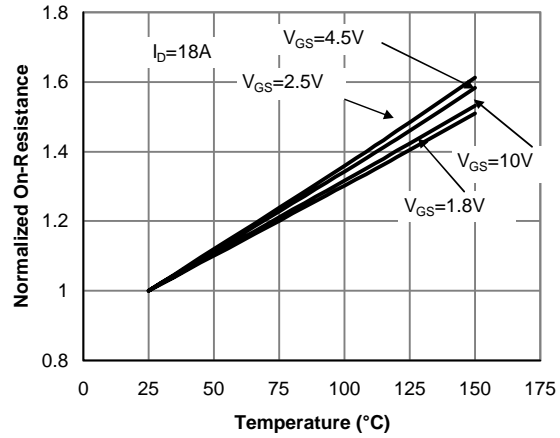


Figure 4: On-Resistance vs. Junction Temperature

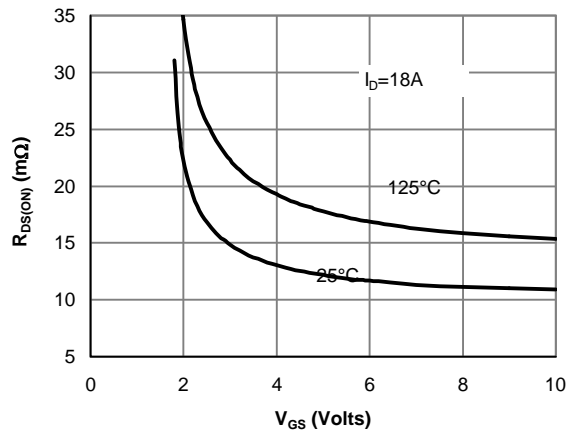


Figure 5: On-Resistance vs. Gate-Source Voltage

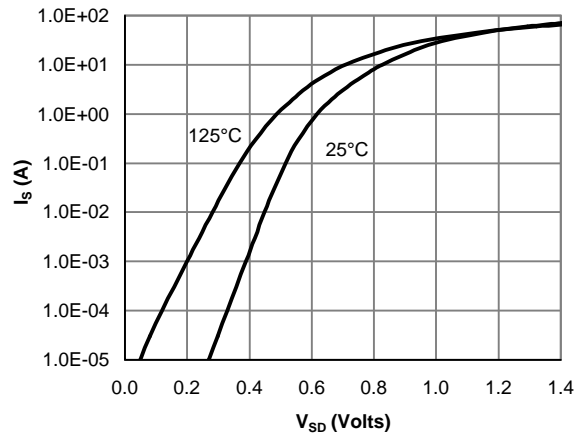


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

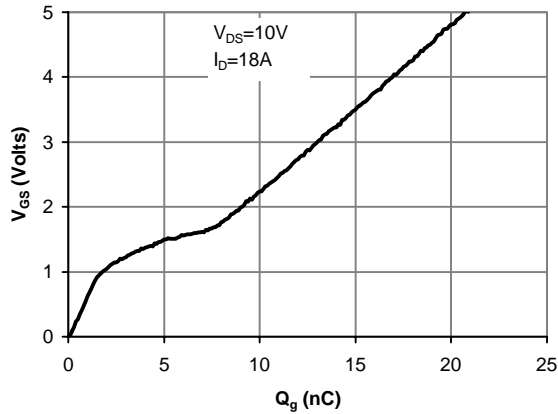


Figure 7: Gate-Charge Characteristics

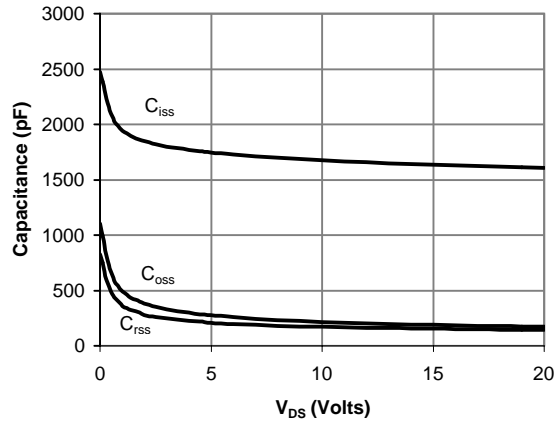


Figure 8: Capacitance Characteristics

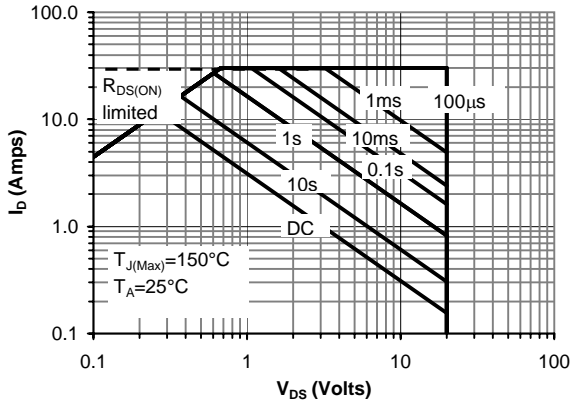


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

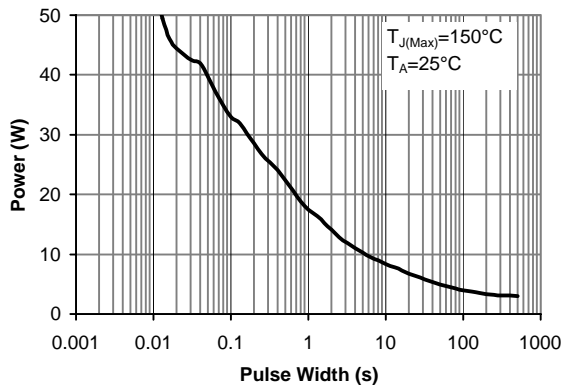


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

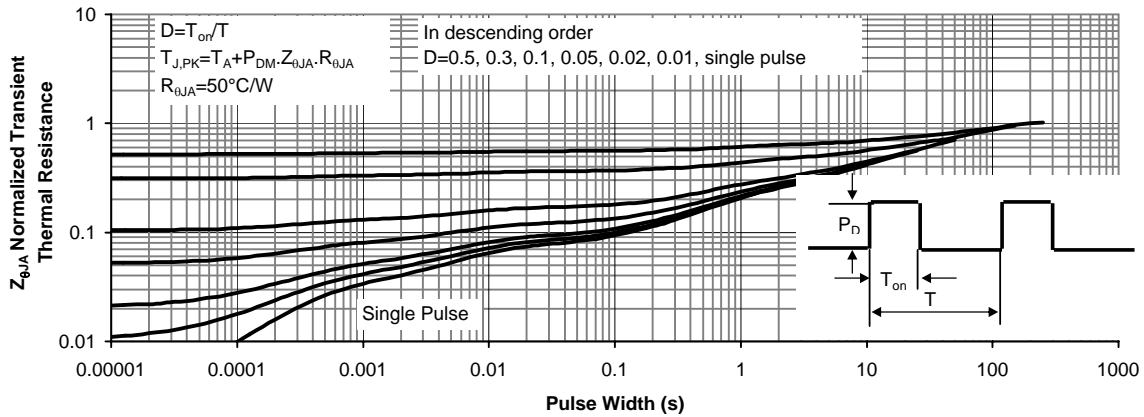


Figure 11: Normalized Maximum Transient Thermal Impedance