

Crystal Oscillators

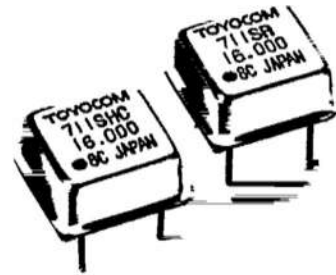
TOYOCOM

CRYSTAL CLOCK OSCILLATORS TCO-700 Series

T-50-23

Features

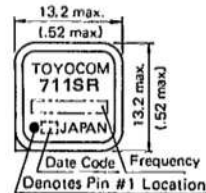
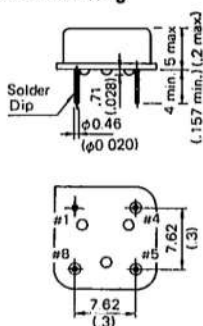
- TTL logic or HCMOS logic outputs
- 8-pin DIP compatible
- Cost and space savings
- Hermetically sealed metal case and high reliability
- Case ground 4-pin for minimizing RF radiation
- Tight symmetry (45 to 55%) available
- Enable/Disable feature available



| Model | | TCO-711S4 | TCO-711SR | TCO-711STH | TCO-711SHC | TCO-711STHC |
|-----------------------------|---|--|--|---|--|--|
| Frequency range | | 1.25 to 50 MHz | | 1.25 to 32 MHz | | |
| Frequency stability* | | | | ±0.01% (±100 ppm) | | |
| Operating temperature range | | 0 to 70°C | | | | |
| Storage temperature range | | -55 to 125°C | | | | |
| Input voltage | | 5.0 V DC ± 10% | | | | |
| Input current | | 30 mA max. (1 to 23 MHz) 50 mA max. (23+ to 50 MHz) | 20 mA max. (1 to 20 MHz) 30 mA max. (20+ to 30 MHz) | | 15 mA max. (C _L = 15 pF) 25 mA max. (C _L = 50 pF) | |
| Output | Symmetry: SYM | 40 to 60% | 45 to 55% (at 1.4V) | 40 to 60% (at 1.4V) | | 40 to 60% (at 50% V _{DD}) |
| | Rise/Fall time: t _r , t _f | 15 ns max. (1 to 9 MHz) 10 ns max. (9+ to 50 MHz) | 5 ns max. | | 6 ns max. (C _L = 15 pF) 12 ns max. (C _L = 50 pF) | |
| | Fanout | 1 to 10 gates, 1.6 mA/gate | | | | I _{OH} = I _{OL} = 4 mA min. |
| Remarks | | TTL logic output | | 3 state output #1 #5 L (GND) "Z" H (open) F ₀ | TTL logic "Z": high impedance tpZL: 100 ns max. tPLZ: 100 ns max. | HCMOS logic output 3 state output |

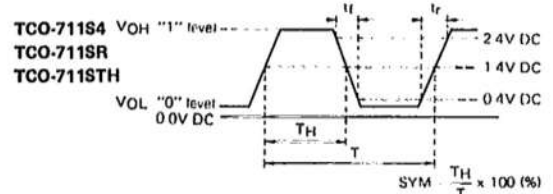
* Inclusive of calibration tolerance at 25°C, operating temperature, input voltage change, load change, aging shock and vibration

Outline drawing

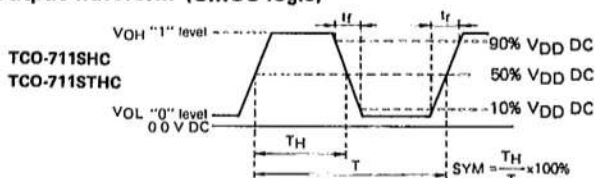


| Pin Connection | | TCO-711S4 | TCO-711STH | TCO-711SHC | TCO-711STHC |
|----------------|----------|-----------|------------|------------|-------------|
| 1 | N C | | CONTROL | | |
| 4 | CASE GND | | | | |
| 5 | OUTPUT | | | | |
| 8 | +V DC | | | | |

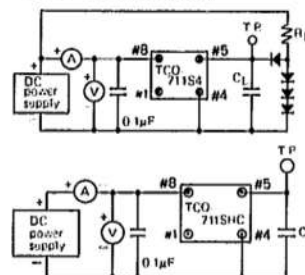
Output waveform (TTL logic)



Output waveform (CMOS logic)



Test circuit diagram



TTL logic output

Note: total fixture and probe capacitance
C_L = 15 pF max.
R_L = 400Ω

CMOS logic output

Note: total fixture and probe capacitance
C_L = 15 pF (or 50 pF max)

Crystal Oscillators

TOYOCOM

SURFACE MOUNT CLOCK OSCILLATORS TCO-700 Series

for devices using microprocessor, personal computer, office computer, facsimile, computer controlled devices, etc.

T-50-23

Features

- TTL logic or HCMOS logic outputs
- Plastic 4 pin SOJ
- Built-in cylinder crystal and high reliability
- Available on 24mm Tape & Reel or in anti-static tube packaging
- Enable/Disable feature available
- Tight symmetry (45 to 55%) available

Absolute maximum ratings

| Parameter | Symbol | Rating | Unit |
|---------------------------|-------------------|-------------|------|
| Supply voltage | $V_{DD} - V_{SS}$ | -0.3 to 7.0 | V |
| Storage temperature range | T_{opr} | -55 to 125 | °C |
| Solder-heat resistance | T_{SOL} | 260 | °C |
| | T | 20 | sec |

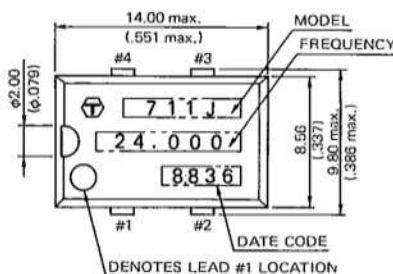


Specifications

| Model | | TCO-711J | TCO-711JC | TCO-711JT | TCO-711JTC |
|-----------------------------|----------------------------|--|--|---|--|
| Frequency range | | 1.5 to 32 MHz ¹ | | | |
| Frequency stability* | | ±0.01% (±100 ppm) | | | |
| Operating temperature range | | 0 to 70°C | | | |
| Input voltage | | +5.0 VDC ± 10% | | | |
| Input current | | 20 mA max. (1.5 to 20 MHz) 30 mA max. (20+ to 32 MHz) | 15 mA max. ($C_L = 15$ pF) 25 mA max. ($C_L = 50$ pF) | 20 mA max. (1.5 to 20 MHz) 30 mA max. (20+ to 32 MHz) | 15 mA max. ($C_L = 15$ pF) 25 mA max. ($C_L = 50$ pF) |
| Output | Symmetry: SYM | 40 to 60% (at 1.4V) | 40 to 60% (at 50% V_{DD}) | 40 to 60% (at 1.4V) | 40 to 60% (at 50% V_{DD}) |
| | Rise/Fall time; t_r, t_f | 15 ns max. (1.5 to 9 MHz) 10 ns max. (9+ to 32 MHz) | 6 ns max. ($C_L = 15$ pF) 12 ns max. ($C_L = 50$ pF) | 15 ns max. (1.5 to 9 MHz) 10 ns max. (9+ to 32 MHz) | 6 ns max. ($C_L = 15$ pF) 12 ns max. ($C_L = 50$ pF) |
| | Fanout | 1 to 10 gates, 1.6 mA/gate | $ I_{OH} = I_{OL} = 4$ mA min. | 1 to 10 gates, 1.6 mA/gate | $ I_{OH} = I_{OL} = 4$ mA min. |
| | Logic | TTL | CMOS | TTL | CMOS |
| Remarks | | | | 3 state output (Enable/Disable) #1 #3 "Z": high impedance L (GND) "Z" tpZL: 100 ns max. H (open) F_0 tpLZ: 100 ns max. | |

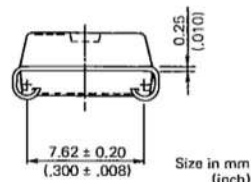
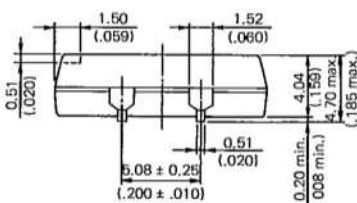
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Outline drawing

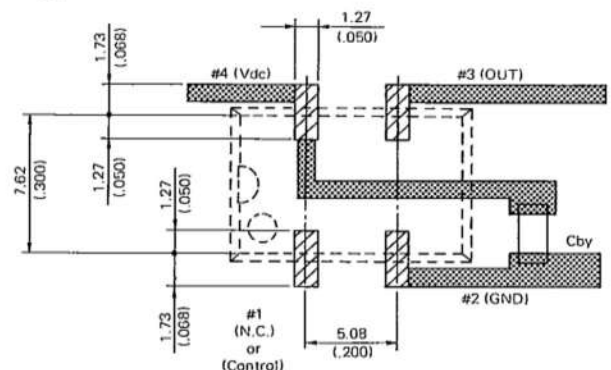


| LEAD | CONNECTION |
|------|-------------------|
| #1 | *N. C. or Control |
| #2 | GND |
| #3 | OUTPUT |
| #4 | +V DC |

*DO NOT use as a tie-point on N. C. models.



Suggested Pads



A near ideal layout of the oscillator is shown at above. The bypass capacitor Cby should be ceramic and 0.1 μ F or greater.