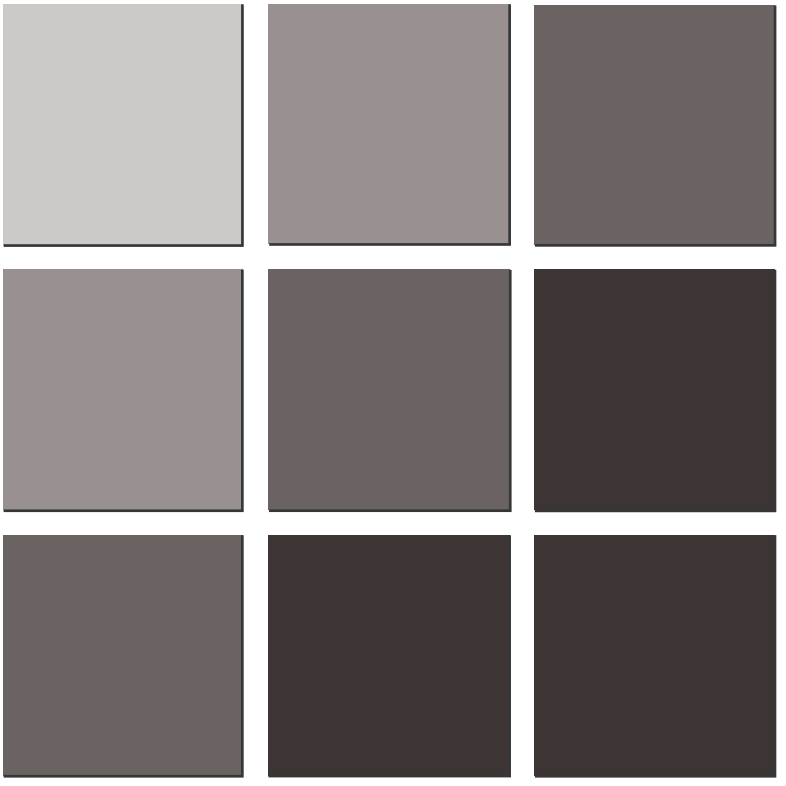
FUJITSU MICROELECTRONICS
PRODUCT GUIDE

PG00-00081-1Ea

2008.1
Product Guide
[ASSP・Memory・ASIC]



FUJITSU

THE POSSIBILITIES ARE INFINITE

Technical Documentation of Electronic Devices

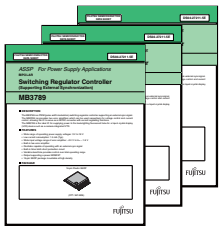
DATA BOOK
(DVD)

PRODUCT GUIDE
(GENERAL)

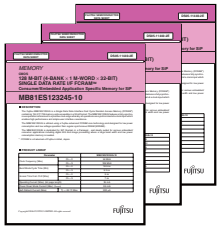
[ASSP·Memory·ASIC]

DATA SHEET

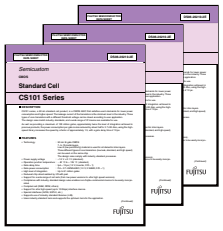
ASSP



Memory

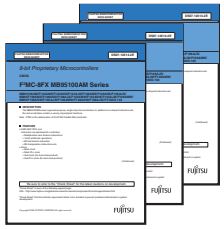


ASIC

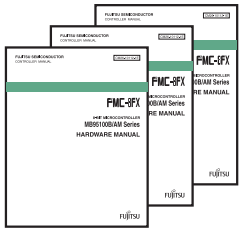


[Microcomputer]

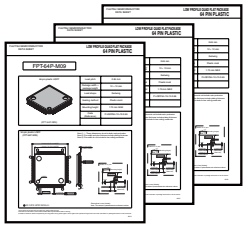
Microcontroller



MANUAL



Package



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*** : SPANSION ™ Products**

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ASSP Product Line-up

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	Telecom		Telephones	2
			Wireless Communication	4
	Communication Control Communication Network	Communication Control	ISDN	18
			IP Packet Processing Engine	18
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	Video Equipment Products		Display Control Products	20
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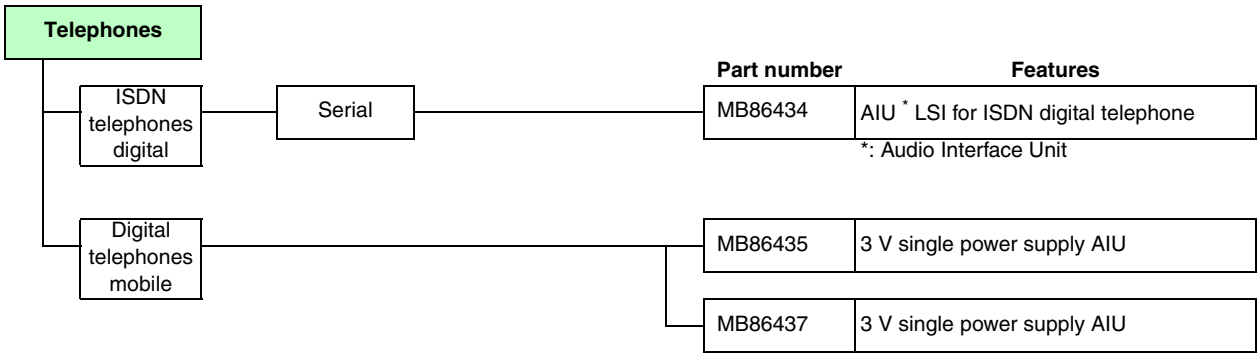
Telephone Products



Part number	Features
MB86434	AIU * LSI for ISDN digital telephone
MB86435	3 V single power supply AIU
MB86437	3 V single power supply AIU

*: Audio Interface Unit

Telephone Products

ISDN Digital Telephone LSIs

Part number	Functions	CODEC	Power supply voltage (V)	Package
				QFP
MB86434	AIU for ISDN digital telephones CODEC, DTMF tones, service tone Internal ringer tone	A-laW μ-laW 14-bit linear	+5±5%	64P

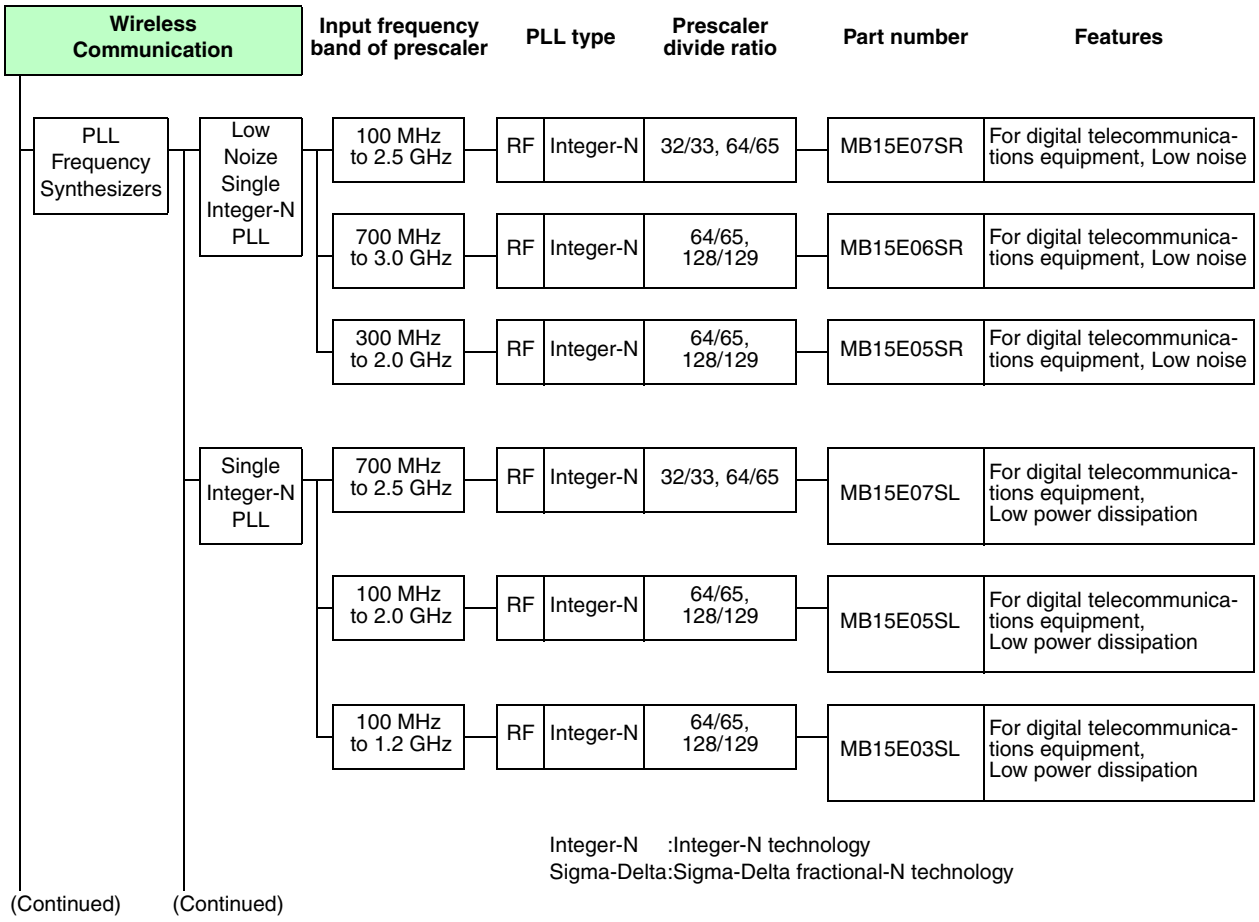
Package: P - Plastic

LSIs for Digital Mobile Telephones

Part number	Functions	Compression law	Power supply voltage (V)	Package
				LQFP
MB86435	3 V single power supply AIU	A-laW μ-laW linear	2.7 to 3.6	64P
MB86437				48P

Package: P - Plastic

Wireless Communication Products



Wireless Communication		Input frequency band of prescaler	PLL type		Prescaler divide ratio	Part number	Features
PLL Frequency Synthesizers	Low Noize Single Integer-N PLL	100 MHz to 2.5 GHz	RF	Integer-N	32/33, 64/65	MB15E07SR	For digital telecommunications equipment, Low noise
		700 MHz to 3.0 GHz	RF	Integer-N	64/65, 128/129	MB15E06SR	For digital telecommunications equipment, Low noise
		300 MHz to 2.0 GHz	RF	Integer-N	64/65, 128/129	MB15E05SR	For digital telecommunications equipment, Low noise
	Single Integer-N PLL	700 MHz to 2.5 GHz	RF	Integer-N	32/33, 64/65	MB15E07SL	For digital telecommunications equipment, Low power dissipation
		100 MHz to 2.0 GHz	RF	Integer-N	64/65, 128/129	MB15E05SL	For digital telecommunications equipment, Low power dissipation
		100 MHz to 1.2 GHz	RF	Integer-N	64/65, 128/129	MB15E03SL	For digital telecommunications equipment, Low power dissipation

Integer-N :Integer-N technology
Sigma-Delta:Sigma-Delta fractional-N technology

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Wireless Communication Products

PLL Frequency Synthesizers

• Low Noize Single Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (µA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC	TSSOP
MB15E07SR	100M	2.5G	Integer -N	32/33, 64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	8.0	0.1	2.7	3.75	5.0	16P	16P
								7.0	0.1	2.7	3.0	5.0		
MB15E06SR	700M	3.0G		64/65, 128/129				8.0	0.1	2.7	3.0	4.0	16P	16P
MB15E05SR	300M	2.0G		64/65, 128/129				7.0	0.1	2.7	3.75	5.0	16P	16P
								6.0	0.1	2.7	3.0	5.0		

Package: P - Plastic

• Single Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (µA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	SSOP	BCC
MB15E07SL	700M	2.5G	Integer -N	32/33, 64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	4.5	0.1	2.4	3.0	3.6	16P	16P
MB15E05SL	100M	2.0G		64/65, 128/129	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	3.5	0.1	2.4	3.0	3.6	16P	16P
MB15E03SL		1.2G		64/65, 128/129	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	2.5	0.1	2.4	3.0	3.6	16P	16P

Package: P - Plastic

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	Input frequency band of prescaler	PLL type		Prescaler divide ratio	Part number	Features
Dual Integer-N PLL	400 MHz to 2.6 GHz	RF	Integer-N	32/33, 64/65	MB15F78UL	For digital telecommunications equipment Low noise Low power dissipation
	100 MHz to 1.2 GHz	IF	Integer-N	16/17, 32/33		
	2.0 GHz to 6.0 GHz	RF	Integer-N	6.0G : 16/17, 32/33	MB15F76UL	For digital high-speed telecommunications equipment
	100 MHz to 1.5 GHz	IF	Integer-N	1.5G : 4/5, 8/9		
				(Fixed part 4 division)		
	2.0 GHz to 4.0 GHz	RF	Integer-N	4.0G : 64/65, 128/129	MB15F74UV	Small Package For digital high-speed telecommunications equipment
	200 MHz to 2.0 GHz	IF	Integer-N	2.0G : 32/33, 64/65		
					MB15F74UL	For digital high-speed telecommunications equipment
	200 MHz to 2.25 GHz	RF	Integer-N	2.25G : 64/65, 128/129	MB15F73UV	Small Package For digital high-speed telecommunications equipment
	50 MHz to 600 MHz	IF	Integer-N	600M : 8/9, 16/17		
					MB15F73UL	For digital high-speed telecommunications equipment
	100 MHz to 1.3GHz	RF	Integer-N	1.3G : 64/65, 128/129	MB15F72UV	Small Package For digital high-speed telecommunications equipment
	50 MHz to 350 MHz	IF	Integer-N	350M : 8/9, 16/17		
					MB15F72UL	For digital high-speed telecommunications equipment
	500 MHz to 2.6 GHz	RF	Integer-N	32/33, 64/65	MB15F30UV	Small Package For digital high-speed telecommunications equipment Low power dissipation
	45 MHz to 510 MHz	IF	Integer-N	8/9, 16/17		
	100 MHz to 1.1GHz	RF	Integer-N	1.1G : 64/65, 128/129	MB15F07SL	For digital high-speed telecommunications equipment Low noise
	100 MHz to 1.1GHz	IF	Integer-N	1.1G : 64/65, 128/129		

Integer-N :Integer-N technology
Sigma-Delta:Sigma-Delta fractional-N technology

(Continued) (Continued)

• Dual Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package	
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC	TSSOP
MB15F74UV	2.0G 200M	4.0G 2.0G	Integer-N	RF : 64/65, 128/129 IF : 32/33, 64/65	Binary 11 bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	6.5 2.5	0.1 0.1	2.7	3.0	3.6	18P	–
MB15F73UV	200M 50M	2.25G 600M		RF : 64/65, 128/129 IF : 8/9, 16/17				2.0 1.2	0.1 0.1	2.4	2.7	3.6	18P	–
MB15F72UV	100M 50M	1.3G 350M		RF : 64/65, 128/129 IF : 8/9, 16/17				1.5 1.0	0.1 0.1	2.4	2.7	3.6	18P	–
MB15F30UV	500M 45M	2.6G 510M		RF : 32/33, 64/65 IF : 8/9, 16/17	Binary 11 bit 3 to 2047	Binary 7bit 0 to 63	Binary 15bit 3 to 32768	2.8 1.2	0.1 0.1	2.4	2.7	3.6	18P	–
MB15F78UL	400M 100M	2.6G 1.2G		RX : 32/33, 64/65 TX : 16/17, 32/33	Binary 11 bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	2.8 1.7	0.1 0.1	2.4	2.7	3.6	20P	20P
MB15F76UL	2.0G 100M	6.0G 1.5G		RF : 16/17, 32/33 (Fixed part 4 division) IF : 4/5, 8/9 (Fixed part 4 division)	Binary 13bit 3 to 8191	Binary 5bit 0 to 31	Binary 14bit 3 to 16383	6.2 2.3	0.1 0.1	2.5	3.0	3.6	20P	–
MB15F74UL	2.0G 200M	4.0G 2.0G		RF : 64/65,128/129 IF : 32/33,64/65	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	6.5 2.5	0.1 0.1	2.7	3.0	3.6	20P	–
MB15F73UL	200M 50M	2.25G 600M		RF : 64/65,128/129 IF : 8/9,16/17				2.0 1.2	0.1 0.1	2.4	2.7	3.6	20P	20P
MB15F72UL	100M 50M	1.3G 350M		RF : 64/65,128/129 IF : 350M: 8/9,16/17				1.5 1.0	0.1 0.1	2.4	2.7	3.6	20P	20P
MB15F07SL	100M 100M	1.1G 1.1G		64/65,128/129 64/65,128/129	Binary 11bit 3 to 2047	Binary 7bit 0 to 127	Binary 14bit 3 to 16383	5.5 5.5	0.1 0.1	2.5	3.0	3.6	16P	16P

Package: P - Plastic

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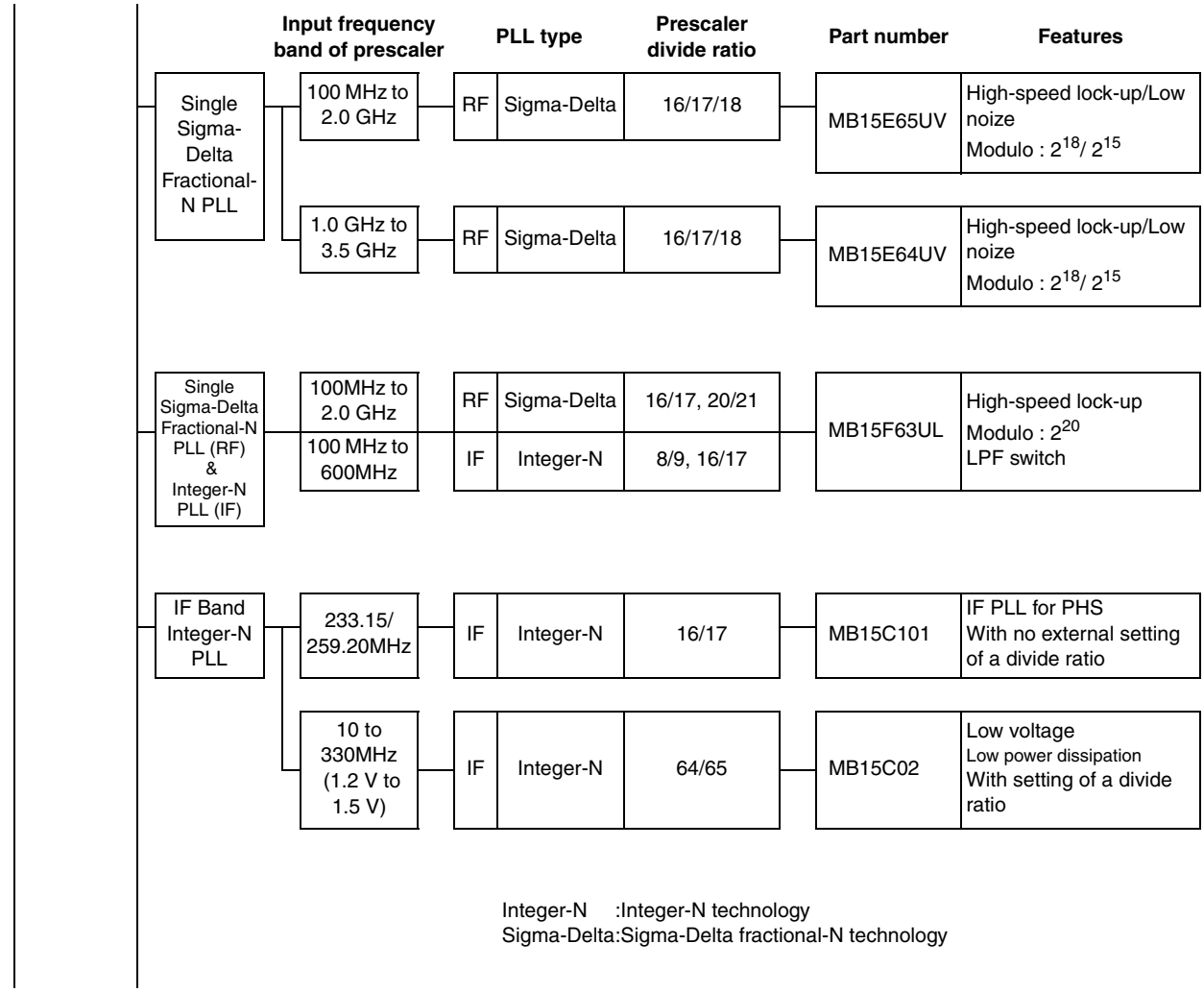

	Input frequency band of prescaler	PLL type		Prescaler divide ratio	Part number	Features
Single Sigma-Delta Fractional-N PLL	100 MHz to 2.0 GHz	RF	Sigma-Delta	16/17/18	MB15E65UV	High-speed lock-up/Low noize Modulo : 2^{18}/ 2^{15}
	1.0 GHz to 3.5 GHz	RF	Sigma-Delta	16/17/18	MB15E64UV	High-speed lock-up/Low noize Modulo : 2^{18}/ 2^{15}
Single Sigma-Delta Fractional-N PLL (RF) & Integer-N PLL (IF)	100MHz to 2.0 GHz	RF	Sigma-Delta	16/17, 20/21	MB15F63UL	High-speed lock-up Modulo : 2^{20} LPF switch
	100 MHz to 600MHz	IF	Integer-N	8/9, 16/17		
IF Band Integer-N PLL	233.15/ 259.20MHz	IF	Integer-N	16/17	MB15C101	IF PLL for PHS With no external setting of a divide ratio
	10 to 330MHz (1.2 V to 1.5 V)	IF	Integer-N	64/65	MB15C02	Low voltage Low power dissipation With setting of a divide ratio

Integer-N :Integer-N technology
Sigma-Delta:Sigma-Delta fractional-N technology

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• Single Sigma-Delta Fractional-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC
MB15E65UV	100 M	2.0 G	Sigma-Delta	16/17/18	Binary 8 bit 9 to 255	Binary 4 bit 0 to 15	Binary 6 bit 1 to 63	4.6	0.1	2.7	3.0	3.3	18P
MB15E64UV	1.0 G	3.5 G		16/17/18	Binary 8 bit 9 to 255	Binary 4 bit 0 to 15	Binary 6 bit 1 to 63	4.6	0.1	2.7	3.0	3.3	18P

Package: P - Plastic

• Single Sigma-Delta Fractional-N PLL (RF) & Integer-N PLL (IF)

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	BCC
MB15F63UL	100M 100M	2.0G 600M	Sigma-Delta, Integer-N	RF : 16/17, 20/21, IF : 8/9,16/17	Binary 7bit 5 to 127(RF) Binary 11bit 3 to 2047(IF)	Binary 4bit 0 to 15(RF) Binary 7bit 0 to 127(IF)	Binary 6bit 1 to 63(RF) Binary 14 bit 3 to 16383(IF)	6.1 1.4	0.1 0.1	2.7	3.0	3.3	20P

Package: P - Plastic

• IF Band Integer-N PLL

Part number	Input frequency band (Hz)		PLL Type	Divide ratio				Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
	min	max		Prescaler	Program counter	Swallow counter	Reference counter			min	typ	max	TSSOP
MB15C101	233.15 259.20		Integer-N	16/17	291 33	7 12	384 40	1.0	–	2.4	3.0	3.6	8P
MB15C02	10 M	330M	Integer-N	64/65	12bit, 5 to 4095	6bit, 0 to 63	14bit, 16 to 16383	1.0	70	1.0	1.2	1.5	16P 20P

Package: P - Plastic

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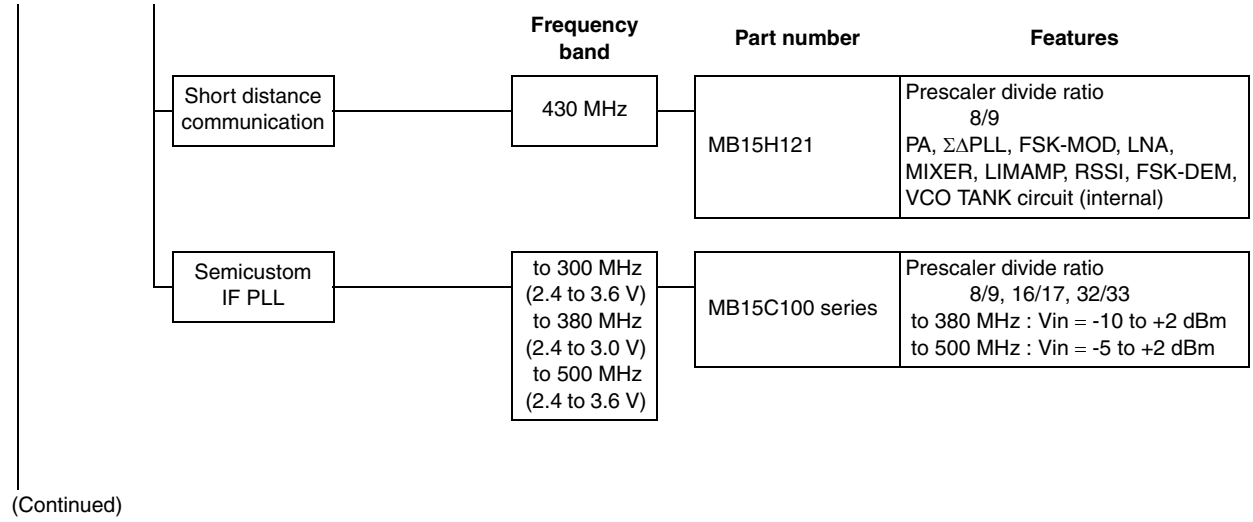

	Frequency band	Part number	Features
Short distance communication	430 MHz	MB15H121	Prescaler divide ratio 8/9 PA, ΣΔPLL, FSK-MOD, LNA, MIXER, LIMAMP, RSSI, FSK-DEM, VCO TANK circuit (internal)
Semicustom IF PLL	to 300 MHz (2.4 to 3.6 V) to 380 MHz (2.4 to 3.0 V) to 500 MHz (2.4 to 3.6 V)	MB15C100 series	Prescaler divide ratio 8/9, 16/17, 32/33 to 380 MHz : Vin = -10 to +2 dBm to 500 MHz : Vin = -5 to +2 dBm

(Continued)

• Specific power saving communication

Part number	Application	Frequency band (MHz)	Functions	Power supply current typ (mA)	Power save current typ (μA)	Power supply voltage (V)			Package
						min	typ	max	LQFP
MB15H121	Telemeter telecontroller security	430	Prescaler divide ratio 8/9 PA, ΣΔPLL, FSK-MOD, LNA, MIXER, LIMAMP, RSSI, FSK-DEM, VCO TANK circuit (internal)	6.7 (PLL) 23.0 (TX) 5.0 (RX)	0.3	2.2	2.5	2.8	48P

Package: P - Plastic

• Semicustom IF PLL

Part number (Series name)	Frequency band (MHz)	Prescaler divide ratio	Power supply current (mA)	Comparison main counter divide ratio (N)	Swallow counter divide ratio (A)	Reference counter divide ratio (R)	Power supply voltage (V)	Package	
								SSOP	BCC
MB15C100 series	to 300 *1 (2.4 to 3.6 V) to 380 *1 (2.4 to 3.0 V) to 500 *2 (2.4 to 3.6 V)	8/9, 16/17, 32/33	1.2 (300 MHz, V_{CC} = 3 V)	Any value between divide-by-5 and divide-by-4095	Any value between divide-by-0 and divide-by-31	Any value between divide-by-5 and divide-by-4095	+2.4 to +3.6	8P	16P (S type)

*1: Input sensitivity –10 to +2 dBm
*2: Input sensitivity –5 to +2 dBm

Package: P - Plastic

Wireless Communication Products

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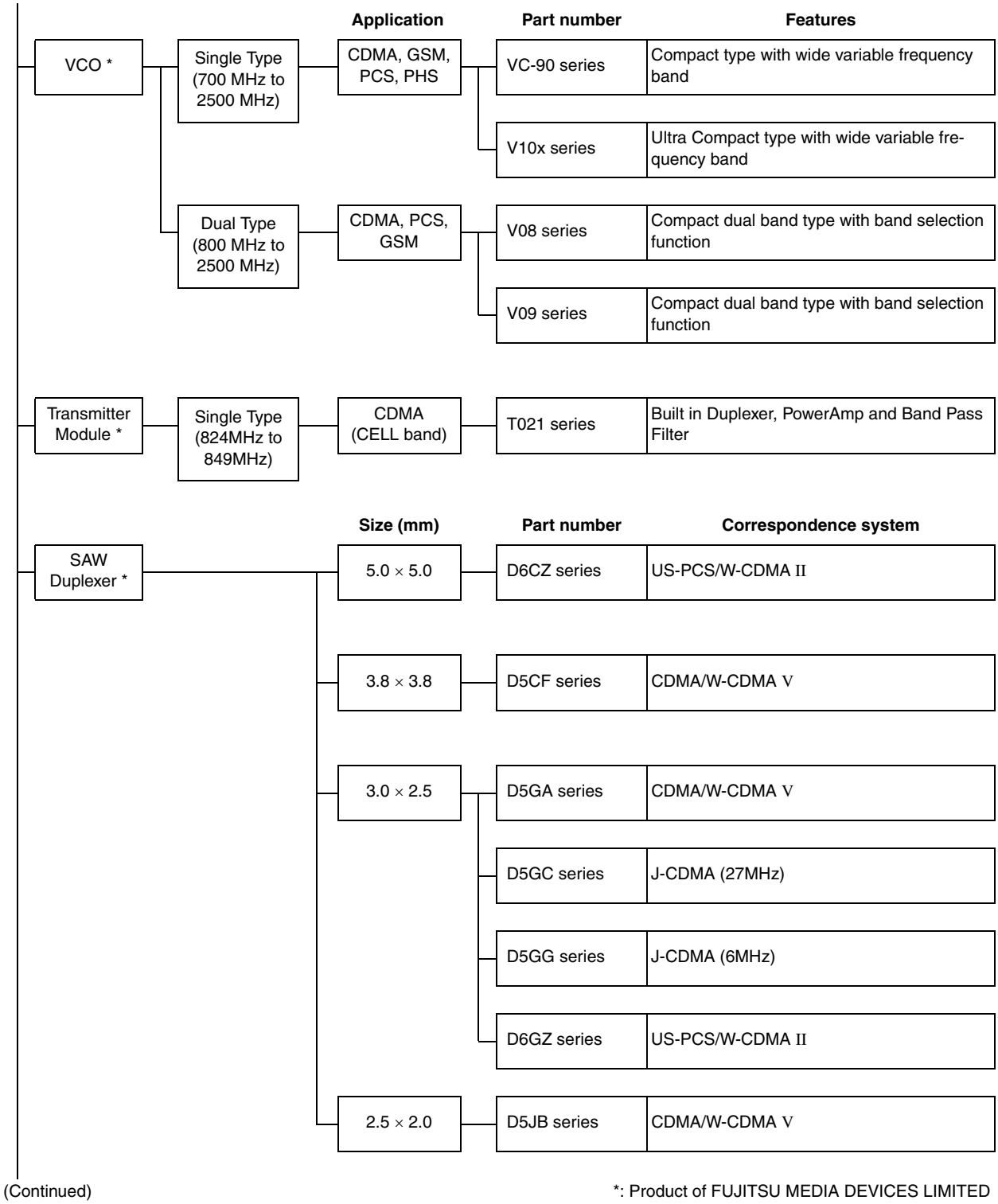

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VCO

Part number	Functions	Application	Frequency (MHz)	Power supply voltage (V)	Package Typ. (mm)
VC-90 series	Voltege Controlled Oscillator	CDMA, GSM, PCS, PHS	700 to 2500	2.5 to 3.3	5.0 × 4.0 × 1.55
V10x series					4.5 × 3.2 × 1.5
V08 series		CDMA, PCS, GSM	800 to 2500	2.8	5.5 × 4.8 × 1.8
V09 series					5.0 × 4.0 × 1.4

(Product of FUJITSU MEDIA DEVICES LIMITED)

Transmitter Module

Part number	Functions	Application	Frequency (MHz)	Power supply voltage (V)	Package Typ. (mm)
T021 series	Built in Duplexer, PowerAmp and Band Pass Filter	CDMA (CELL band)	824 to 849	3.4	8.0 × 5.0 × 1.4

(Product of FUJITSU MEDIA DEVICES LIMITED)

SAW Duplexer for Mobile Communication System

Correspondence system	Size (mm)	Part Number	Remarks
CDMA/W-CDMA V	3.8 × 3.8	FAR-D5CF-881M50-D1F1	Two types of package are available
	3.0 × 2.5	FAR-D5GA-881M50-D1AA	Two types of package are available
	2.5 × 2.0	FAR-D5JB-881 M50-D3AA	Two types of package are available
J-CDMA (27MHz)	3.0 × 2.5	FAR-D5GC-911M50-D1CA	-
J-CDMA (6MHz)	3.0 × 2.5	FAR-D5GG-872M00-D1GA	-
US-PCS/W-CDMA II	5.0 × 5.0	FAR-D6CZ-1G9600-D1XC	Two types of package are available
	3.0 × 2.5	FAR-D6GZ-1G9600-D1ZA	Two types of package are available

(Product of FUJITSU MEDIA DEVICES LIMITED)

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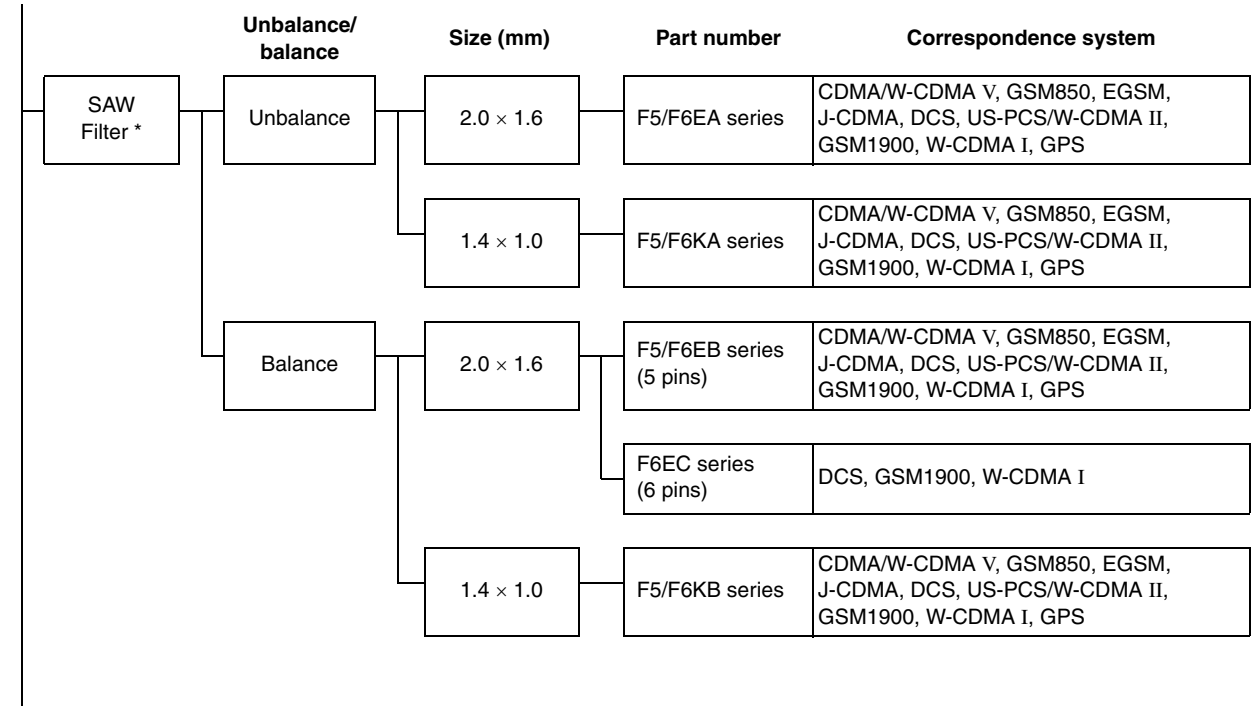

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*: Product of FUJITSU MEDIA DEVICES LIMITED

SAW Filter for Mobile Communication System

Correspondence system	Transmission/ Reception	Size (mm)	Part number	Remarks
CDMA/W-CDMA Ⅴ, GSM850	Transmission	2.0 × 1.6	FAR-F5EA-836M50-D27A	Unbalanced
		1.4 × 1.0	FAR-F5KA-836M50-D4DF	Unbalanced
			FAR-F5KB-836M50-B4EG	Balanced 200 ohm output
	Reception	2.0 × 1.6	FAR-F5EA-881M50-D27B	Unbalanced
			FAR-F5EB-881M50-B2JJ	5 pins, Balanced 100 ohm output
			FAR-F5EB-881M50-B28W	5 pins, Balanced 150 ohm output
		1.4 × 1.0	FAR-F5KA-881M50-D4CH	Unbalanced
			FAR-F5KB-881M50-B4ED	Balanced 100 ohm output
			FAR-F5KB-881M50-B4EA	Balanced 150 ohm output
			FAR-F5KB-881M50-B4EM	Balanced 150 ohm output
EGSM	Transmission	2.0 × 1.6	FAR-F5EA-897M50-D27C	Unbalanced
		1.4 × 1.0	FAR-F5KA-897M50-D4DC	Unbalanced
	Reception	2.0 × 1.6	FAR-F5EA-942M50-D27F	Unbalanced
			FAR-F5EB-942M50-B28E	5 pins, Balanced 150 ohm output
		1.4 × 1.0	FAR-F5KA-942M50-D4CJA	Unbalanced
			FAR-F5KB-942M50-B4EB	Balanced 150 ohm output
J-CDMA (32MHz)	Reception	1.4 × 1.0	FAR-F5KB-859M00-B4EE	Balanced 100 ohm output
GPS	-	2.0 × 1.6	FAR-F6EA-1G5754-L2AZ	Unbalanced
			FAR-F6EB-1G5754-B2BS	5 pins, Balanced 100 ohm output
		1.4 × 1.0	FAR-F6KA-1G5754-L4AA	Unbalanced
			FAR-F6KA-1G5754-L4AJ	Uubalanced
			FAR-F6KB-1G5754-B4GE	Balanced 100 ohm output, Low loss
			FAR-F6KB-1G5754-B4GU	Balanced 100 ohm output, High Attenuation
DCS	Reception	2.0 × 1.6	FAR-F6EA-1G8425-D2ABA	Unbalanced
			FAR-F6EB-1G8425-B2BG	5 pins, Balanced 150 ohm output
			FAR-F6EC-1G8425-B2CE	6 pins, Balanced 150 ohm output
		1.4 × 1.0	FAR-F6KA-1G8425-D4CK	Unbalanced
			FAR-F6KB-1G8425-B4GA	Balanced 150 ohm output
US-PCS/W-CDMA Ⅱ, GSM1900	Transmission	2.0 × 1.6	FAR-F6EA-1G8800-L2AN	For Full Band
		1.4 × 1.0	FAR-F6KA-1G8800-L4AF	For Full Band
	Reception	2.0 × 1.6	FAR-F6EA-1G9600-D2AC	Unbalanced
			FAR-F6EB-1G9600-B2BK	5 pins, Balanced 100 ohm output
			FAR-F6EB-1G9600-B2BW	5 pins, Balanced 150 ohm output
			FAR-F6EC-1G9600-B2CW	6 pins, Balanced 150 ohm output
		1.4 × 1.0	FAR-F6KA-1G9600-D4CR	Unbalanced
			FAR-F6KB-1G9600-B4GP	Balanced 100 ohm output
			FAR-F6KB-1G9600-B4GB	Balanced 150 ohm output
W-CDMA Ⅰ	Transmission	2.0 × 1.6	FAR-F6EA-1G9500-D2AL	Unbalanced
		1.4 × 1.0	FAR-F6KA-1G9500-D4CD	Unbalanced
			FAR-F6KA-1G9500-D4DG	Unbalanced
			FAR-F6KB-1G9500-B4GJ	Balanced 100 ohm input
	Reception	2.0 × 1.6	FAR-F6EB-2G1400-B2BN	5 pins, Balanced 100 ohm output
			FAR-F6EC-2G1400-B2CP	6 pins, Balanced 200 ohm output
		1.4 × 1.0	FAR-F6KA-2G1400-D4CG	Unbalanced
			FAR-F6KB-2G1400-B4GC	Balanced 100 ohm output
			FAR-F6KB-2G1400-B4GD	Balanced 200 ohm output

(Product of FUJITSU MEDIA DEVICES LIMITED)

Wireless Communication Products

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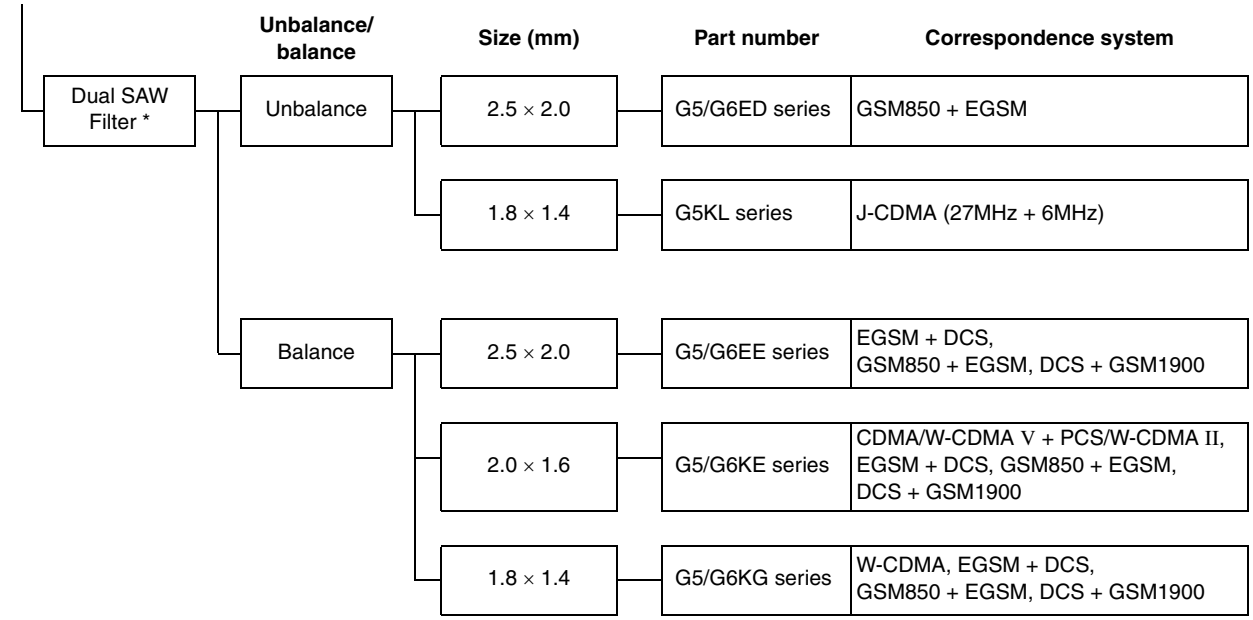


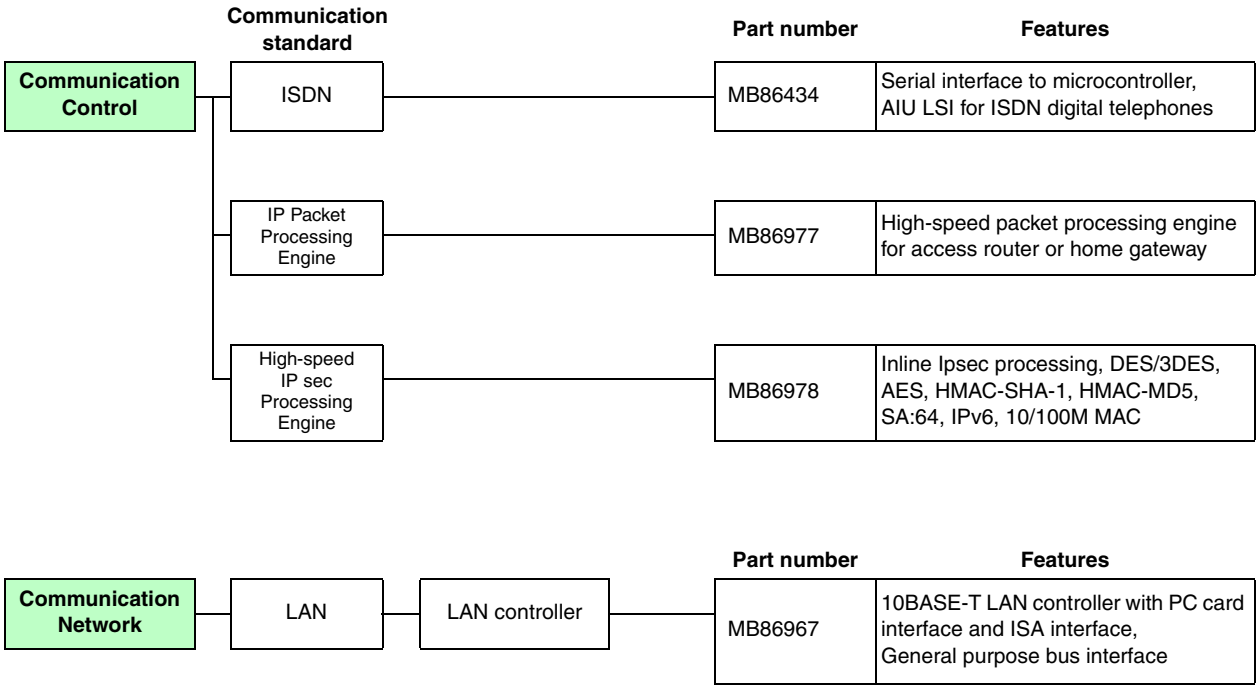
*: Product of FUJITSU MEDIA DEVICES LIMITED

SAW Dual Filter for Mobile Communication System

Correspondence system	Transmission/ Reception	Size (mm)	Part number	Remarks
EGSM + DCS	Reception	2.5 × 2.0	FAR-G6EE-1G8425-Y2PN	Balanced 150 ohm output, Opposite type of Filter position is available.
		2.0 × 1.6	FAR-G6KE-1G8425-Y4QG	Balanced 150 ohm output, Opposite type of Filter position is available.
		1.8 × 1.4	FAR-G6KG-1G8425-Y4SA	Balanced 150 ohm output, Opposite type of Filter position is available.
GSM850 + EGSM	Transmission	2.5 × 2.0	FAR-G5ED-897M50-D2DE	Unbalanced
	Reception	2.5 × 2.0	FAR-G5EE-942M50-Y2PB	Balanced 150 ohm output, Opposite type of Filter position is available.
		2.0 × 1.6	FAR-G5KE-942M50-Y4QA	Balanced 150 ohm output, Opposite type of Filter position is available.
		1.8 × 1.4	FAR-G5KG-942M50-Y4SD	Balanced 150 ohm output, Opposite type of Filter position is available.
DCS + GSM1900	Reception	2.5 × 2.0	FAR-G6EE-1G9600-Y2PR	Balanced 150 ohm output, Opposite type of Filter position is available.
		2.0 × 1.6	FAR-G6KE-1G9600-Y4QB	Balanced 150 ohm output, Opposite type of Filter position is available.
		1.8 × 1.4	FAR-G6KG-1G9600-Y4SC	Balanced 150 ohm output, Opposite type of Filter position is available.
CDMA/W-CDMA V + US-PCS/W-CDMA II	Reception	2.0 × 1.6	FAR-G6KE-1G9600-Y4LY	Balanced 100 ohm output
J-CDMA (27 MHz + 6 MHz)	Transmission	1.8 × 1.4	FAR-G5KL-911M50-D4XA	Unbalanced, 1input/2output
W-CDMA I + V	Transmission	1.8 × 1.4	FAR-G6KG-1G9500-Y4PG	Balanced 200 ohm input
	Reception	1.8 × 1.4	FAR-G6KG-2G1400-Y4SH	Balanced 200 ohm output

(Product of FUJITSU MEDIA DEVICES LIMITED)

Communication Control/Communication Network



Communication Control

ISDN

Part number	Functions	Communication standard	Power supply voltage (V)	Package
				QFP
MB86434	AIU LSI for ISDN digital telephones, Internal CODEC, DTMF tones, service tone, and ringer tone	-	+5 ± 5%	64P

Package: P - Plastic

IP Packet Processing Engine

Part number	Functions	Power supply voltage (V)	Package
			LQFP
MB86977	Enable to process following functions with hardware. IP Packet Forwarding Packet Filtering NAT PPPoE and more. Supports QoS, DMZ, IPv6 and more. 10/100M MAC (Conforms to IEEE802.3)	3.3 ± 0.3 1.8 ± 0.15	208P

Package: P - Plastic

High Speed IP sec Processing Engine

Part number	Functions	Power supply voltage (V)	Package
			FBGA
MB86978	Inline Ipsec processing, DES / 3DES,AES,HMAC - SHA-1,HMAC-MD5,SA:64,IPv6,10 / 100M MAC	3.3 ± 0.3 1.8 ± 0.15	337P 288P

Package: P - Plastic

Communication Network

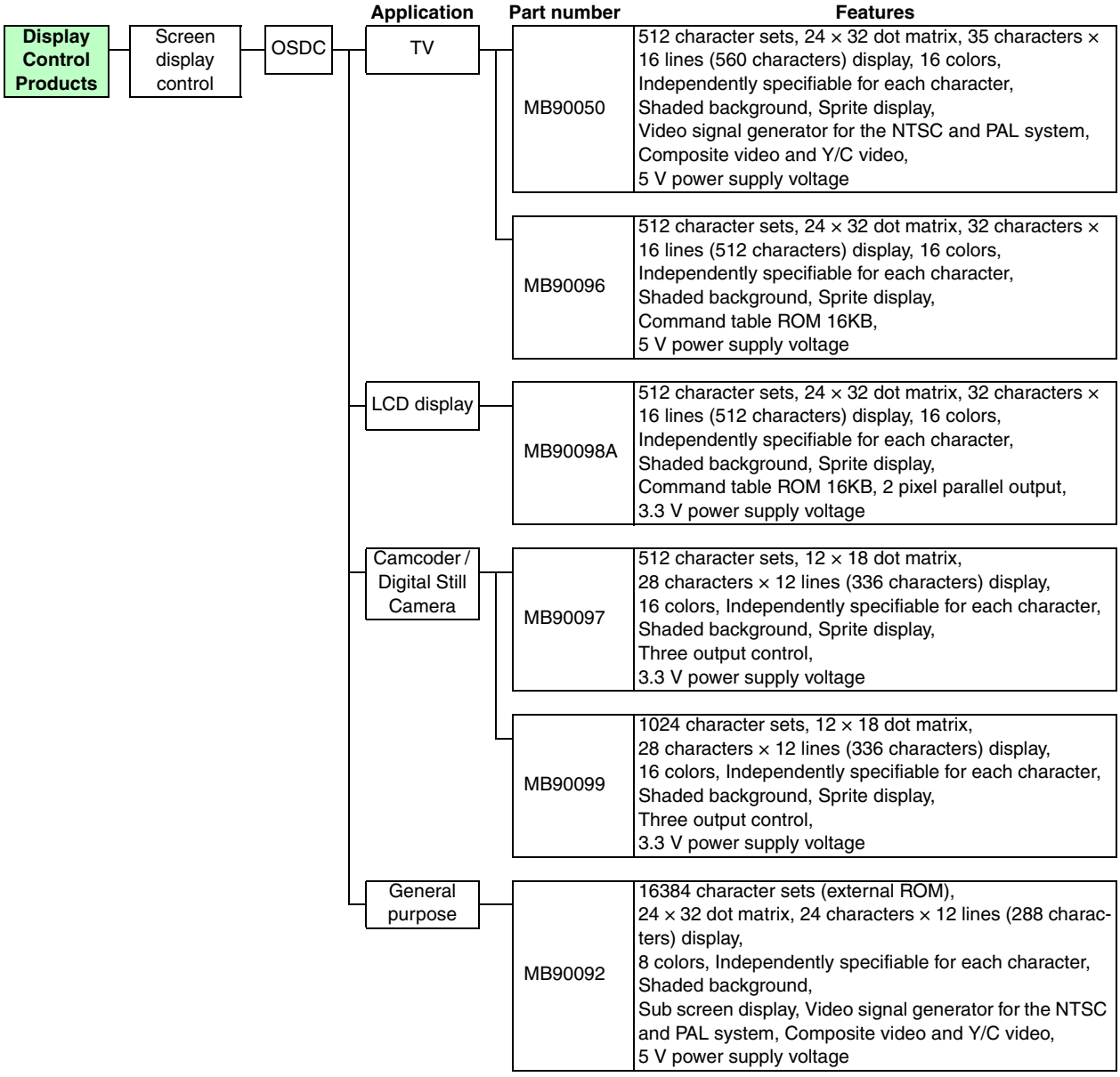
LAN

Part number	Functions	Communication standard	Power supply voltage (V)	Package
				LQFP
MB86967	10BASE-T Ethernet controller with PC card interface, ISA bus interface and General purpose bus interface	Conforms to IEEE 802.3	+5 ± 5%	100P

Note: Ethernet is a registered trademark of XEROX Corporation of the USA.

Package: P - Plastic

Display Control Products



Display Control Products

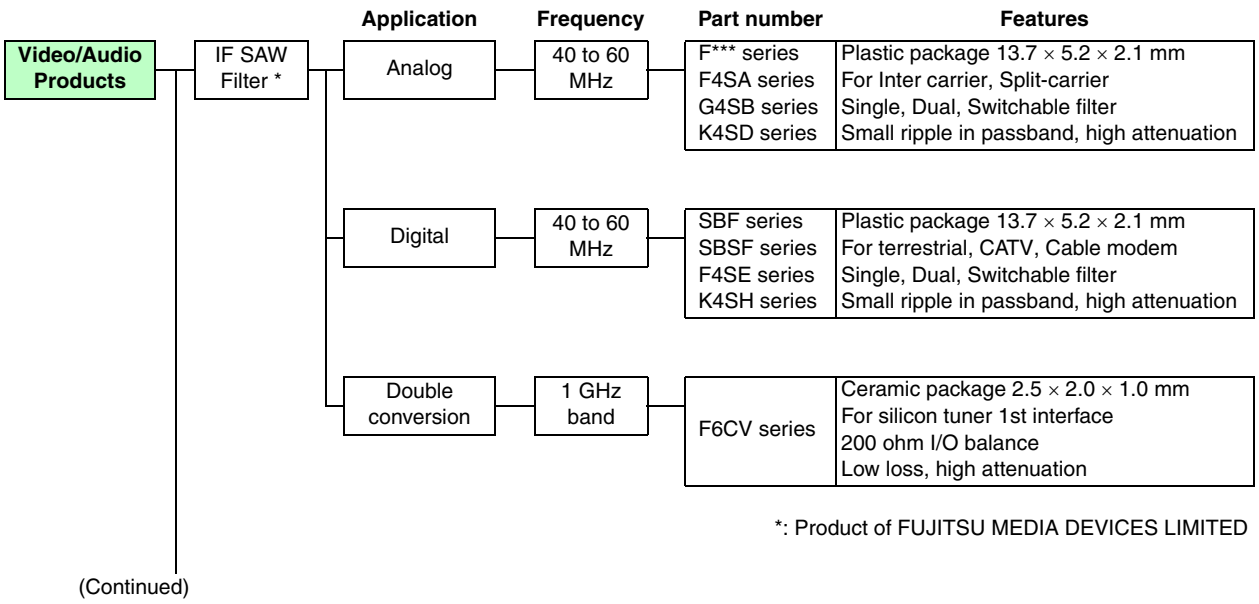
Screen Display Control

OSDC (On-Screen Display Controller)

Part number	Character generator	Number of character set	Character dot structure	Screen size	RGB digital output	Analog (video) output	Sync signal generation	Power supply voltage (V)	Package				
									SH-DIP	SOP	QFP	SSOP	FLGA
MB90050	Internal ROM	512	24 × 32	35 characters × 16 lines	6bit (16 color selection in 64 colors)	Composite Video and Y/C video	NTSC PAL	+5 ±10%	—	—	48P	—	—
MB90096	Internal ROM	512	24 × 32	32 characters × 16 lines	4bit (16 colors)	Unavailable	Unavailable	+5 ±10%	28P	28P	—	—	—
MB90098A	Internal ROM	512	24 × 32	32 characters × 16 lines	4bit (16 colors)	Unavailable	Unavailable	+3.3 ±0.3	—	28P	—	—	—
MB90097	Internal ROM	512	12 × 18	28 characters × 12 lines	4bit (16 colors)	Unavailable	Unavailable	+3.3 ±0.3	—	—	—	20P	—
MB90099	Internal ROM	1024	12 × 18	28 characters × 12 lines	4bit (16 colors)	Unavailable	Unavailable	+2.4 to +3.6	—	—	—	20P	20P
MB90092	External ROM	16384 (Max.)	24 × 32	24 characters × 12 lines	3bit (8 colors)	Composite Video and Y/C video	NTSC PAL	+5 ±10%	—	—	80P	—	—

Package: P - Plastic

Video/Audio Products



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Video/Audio Products

IF SAW Filter for Analog

(Product of FUJITSU MEDIA DEVICES LIMITED)

Applicable types	System	Video/Audio	Picuture carrier frequency (MHz)	Part number
NTSC N	Inter-Carrier (single)	Video	58.75	F081EPL
	Split-Carrier (single)	Video	58.75	FAR-F4SA-58M750-A008
	Split-Carrier (single)	Video	58.75	FAR-F4SA-58M750-A019
	Split-Carrier (single)	Audio	58.75	FAR-F4SA-54M250-B011
	Split-Carrier (dual)	Video/Audio	58.75	FAR-G4SB-58M750-D018
NTSC M/N	Inter-Carrier (single)	Video	45.75	F072TPL-A
	Split-Carrier (single)	Video	45.75	FAR-F4SA-45M750-A024
	Split-Carrier (single)	Audio	45.75	FAR-F4SA-41M250-B021
	Split-Carrier (dual)	Video/Audio	45.75	FAR-G4SB-45M750-D025
PAL B/G/D/K/I	Inter-Carrier (single)	Video	38.90	FAR-F4SA-38M900-A041
	Split-Carrier (single)	Video	38.90	FAR-F4SA-38M900-A071
	Split-Carrier (single)	Video	38.90	FAR-F4SA-38M900-A072
	Split-Carrier (single)	Audio	38.00	F337MPL
	Split-Carrier (single)	Audio	38.90	FAR-F4SA-40M400-B071
PAL B/G, D/K, NTSC M/N	Split-Carrier (Switchable)	Video + Video	38.00	FAR-K4SD-38M000-F002
	Split-Carrier (Switchable)	Video + Video	38.00	FAR-K4SD-38M000-F011
	Split-Carrier (Switchable)	Video + Video	38.90	FAR-K4SD-38M900-F003
PAL D/K/I, B/G, L/L'	Split-Carrier (Switchable)	Audio + Audio	33.90/38.90	FAR-K4SD-40M400-G001
	Split-Carrier (Switchable)	Audio + Audio	33.90/38.90	FAR-K4SD-40M400-G002
	Split-Carrier (Switchable)	Audio + Audio	33.90/38.90	FAR-K4SD-40M400-G031
	Split-Carrier (dual)	Audio + Audio	33.90/38.90	F817JPL

IF SAW Filter for Digital

(Product of FUJITSU MEDIA DEVICES LIMITED)

Applicable types	Center frequency (MHz)	3 dB Bandwidth (MHz)	Part number
DAB	38.912	1.50	SBF0402GPL
OOB	44.000	1.70	SBF0402JPL
	44.000	1.70	FAR-F4SE-44M000-A011
	44.000	2.60	FAR-F4SE-44M000-H0A6
	44.000	4.00	FAR-F4SE-44M000-H0A3
CATV/TV (US/Euro)	36.000	8.10	FAR-F4SE-36M000-A005
	36.125	6.10	FAR-F4SE-36M125-A001
	36.125	7.00	SBF0407BPL
	36.125	8.10	SBF0408KPL
	43.750	6.00	FAR-F4SE-43M750-A006
	43.750	6.00	FAR-F4SE-43M750-H0AB
	44.000	5.35	FAR-F4SE-44M000-H0AG
	44.000	5.37	FAR-F4SE-44M000-H0A4
	44.000	5.42	FAR-F4SE-44M000-H0A8
	44.000	5.49	FAR-F4SE-44M000-H0A1
	44.000	5.50	FAR-F4SE-44M000-H0AH
	44.000	6.00	FAR-F4SE-44M000-H0A9
	44.000	6.12	FAR-F4SE-44M000-H0A2
	44.000	6.20	FAR-F4SE-44M000-H0AA
	44.000	8.00	SBF0408LPL
	47.250	6.20	FAR-F4SE-47M250-H0AC
	36.000	6.4/7.4 (Switchable)	FAR-K4SH-36M000-L0E1
	36.000	7.0/7.9 (Switchable)	SBSF03ABPL
	36.125	6.0/7.9 (Switchable)	FAR-K4SH-36M125-F001
	36.125	7.0/7.9 (Switchable)	SBSF03AAPL
CATV/TV (Japan)	57.000	5.30	FAR-F4SE-57M000-H0JC
	57.000	5.40	FAR-F4SE-57M000-H0J9
	57.000	5.62	FAR-F4SE-57M000-H0J6
	57.000	5.62	FAR-F4SE-57M000-H0J3
TV tuner	35.230	8.00	FAR-F4SE-35M230-A013
	36.125	6.90	FAR-F4SE-36M125-H0E8
	36.125	7.60	FAR-F4SE-36M125-H0E5
TV/STB	36.125	7.90	FAR-F4SE-36M125-H0E7

IF SAW Filter for Double Conversionl

(Product of FUJITSU MEDIA DEVICES LIMITED)

Applicable types	Center frequency (MHz)	Bandwidth (MHz)	Part number
1st IF	1220.000	8.00	FAR-F6CV-1G2200-C27A

Video/Audio Products/Demodulator Products

(Continued)

	Application	Capacity	Organization	Part number	Features
EDID memory	DTV/display for HDMI	2K-bit	256 × 8	MB85RF402	For 4 DDC(I^2C) ports

	Application	Part number	Features
Digital Demodulator	Satellite	MB86667	Small 48 pin package High tolerance to spectrum distortion High and stability of reception Blind Scan support
	Cable	MB86668	Small 48 pin package High tolerance to spectrum distortion High and stability of reception
	Ground Wave	MB86A20	Support Japanese Terrestrial Digital TV and Digital Radio. All memory such as time-interleave is implemented. Input signal : 4MHz-IF or 57MHz-IF Output signal : serial or parallel TS

EDID memory

Part Number	Memory	Organization (W × b)	Interface	Supply Voltage (V)	Packages
					TSSOP
○MB85RF402	FRAM	256 × 8	For 4 DDC(I^2C) ports	3.8 to 5.5	16P

○ : New released. Pakage : P - Plastic

Demodulator Products

Satellite

Part number	Function	Power supply voltage (V)	Package
			QFP
MB86667	QPSK demodulator DVB-S and DSS support	1.65 to 1.95 3.0 to 3.6	48P

Package: P - Plastic

Cable

Part number	Function	Power supply voltage (V)	Package
			QFP
MB86668	QAM demodulator DVB-C support	1.65 to 1.95 3.0 to 3.6	48P

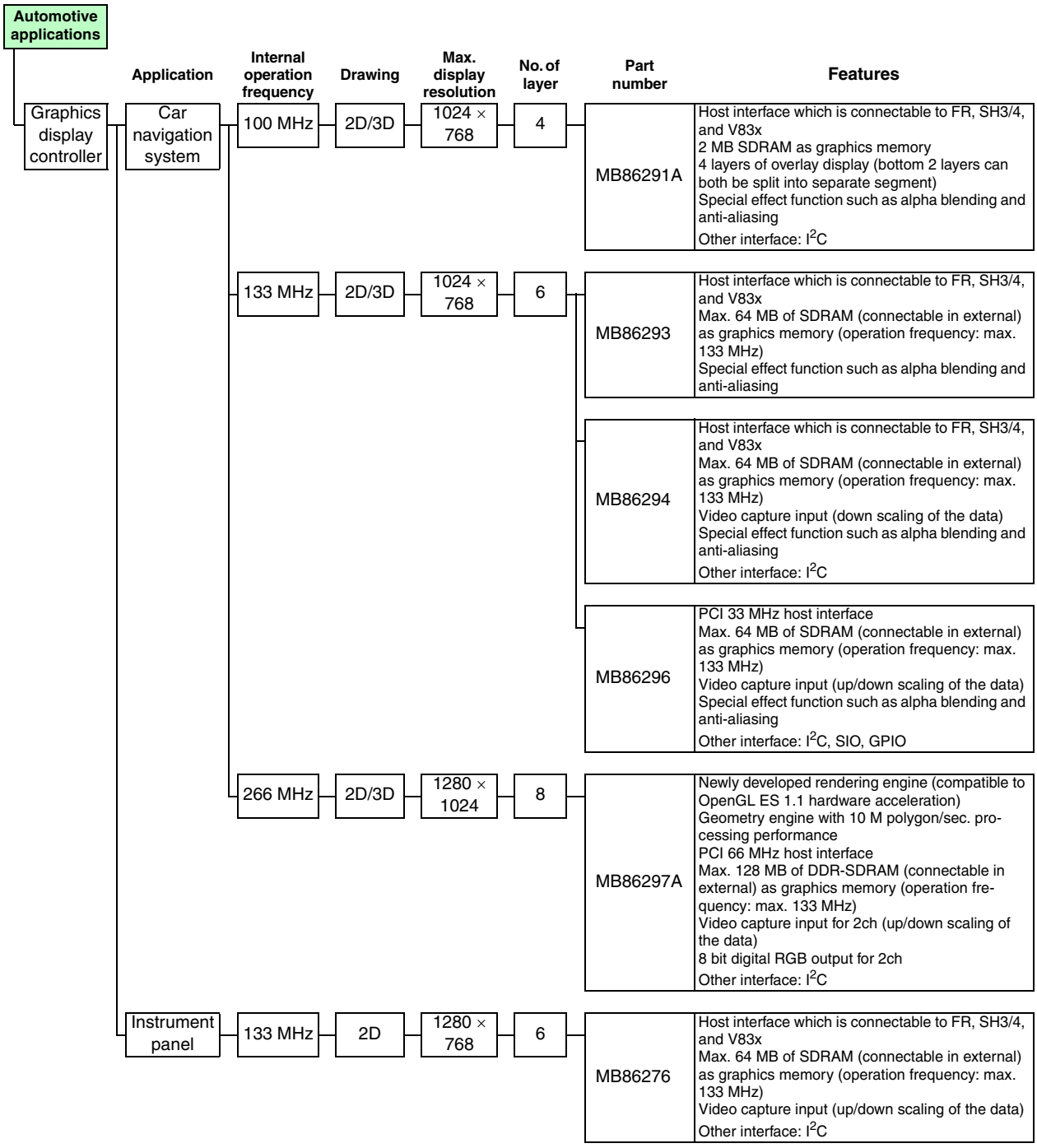
Package: P - Plastic

Ground Wave

Part number	Function	Power supply voltage (V)	Package
			FBGA
MB86A20	13 segment OFDM demodulator ISDB-T support	1.4 to 1.6 1.65 to 1.95 3.0 to 3.6	144P

Package: P - Plastic

Automotive Applications



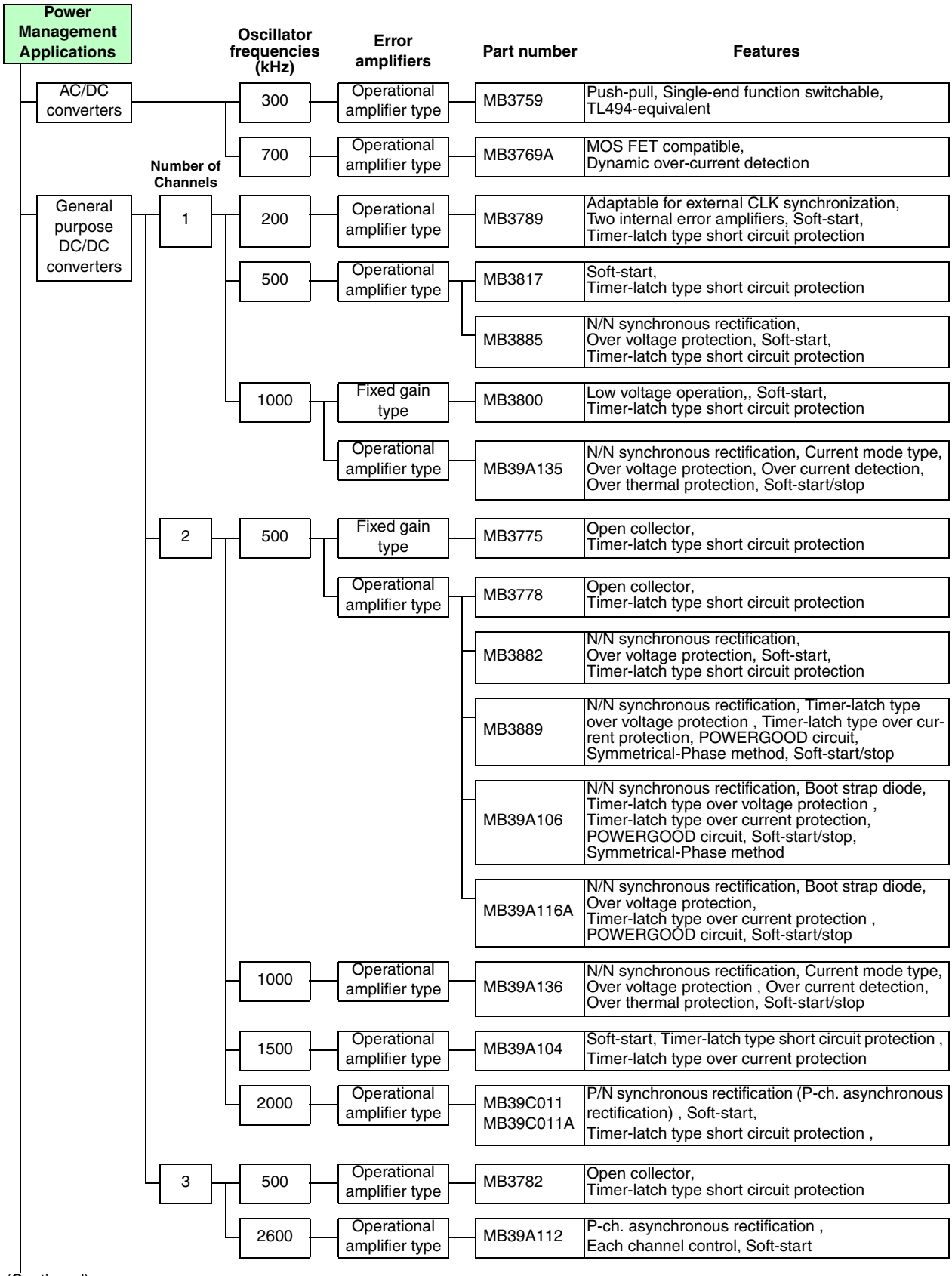
Automotive Applications

Graphics Display Controller

Part number	Internal operation frequency	Rendering engine	Geometry engine	Max. graphics memory	Drawing	Display resolution (pixel)	No. of layer	Texture mapping (pixel)	Video capture input	Video scaling	Video output	Host interface	Power supply voltage (standard value)	Operation temp. range (°C)	Package
MB86291A	100 MHz	Built-in	Built-in	2 MB SDRAM (built-in)	2D/3D	Max. 1024 × 768	4	Max. 256 × 256	YUV	-	RGB analog/ digital	32 bit parallel	I/O: 3.3 V Internal: 2.5 V	-30 to +85	QFP-208P
MB86293	133 MHz			64 MB SDRAM (external)			6 (included 1 alpha plane)	Max. 4096 × 4096	-	-	RGB digital		I/O: 3.3 V Internal: 1.8 V	-40 to +85	QFP-256P
MB86294									YUV	Down	RGB analog/ digital				QFP-256P BGA-256P
MB86296									YUV/ RGB	Up/ Down		PCI 33 MHz			BGA-256P
MB86297A	266 MHz			128 MB DDR-SDRAM (external)		Max. 1280 × 1024	8 (plus 4 alpha plane)		YUV × 2/ RGB + YUV	Up/ Down	RGB digital × 2	PCI 66 MHz	I/O: 3.3 V Internal: 1.2 V		TEBGA-543P
MB86276	133 MHz		-	64 MB SDRAM (external)	2D	Max. 1280 × 768	6 (included 1 alpha plane)		YUV/ RGB	Up/ Down	RGB digital	32/16 bit parallel Address/ data bus multiplex	I/O: 3.3 V Internal: 1.8 V		PBGA-320P

Packages: P - Plastic

Power Management Applications



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Power Management Applications

AC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage (V) (Typ.)	Reference voltage Precision (%)	Package SOP
MB3759	PWM-type controllers for AC/DC converters	+7 to +32	1	300	5	5.0	16P
MB3769A		+12 to +18		700		2.0	16P

Packages: P - Plastic

General Purpose DC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage (V) (Typ.)	Reference voltage Precision (%)	Solutions	Package SOP	Package SSOP	Package TSSOP
MB3789	PWM-type controllers for DC/DC converters	+3.0 to +18	1	200	2.5	4.0	Up conversion	–	16P	–
MB3817		+2.5 to +18		500	1.5	2.0	Up conversion Down conversion Invert	–	16P	–
MB3885		+5.5 to +18			1.25	1.0	Down conversion	–	20P	–
MB3800		+1.8 to +15		1000	0.5	4.0	Up conversion	8P	8P	–
○MB39A135		+4.5 to +25			0.7	1.0	Down conversion	–	–	24P
MB3775	PWM-type controllers for DC/DC converters	+3.6 to +18	2	500	1.28	1.5	Up conversion Down conversion Invert	16P	16P	–
MB3778					2.46	2.0		16P	16P	–
MB3882		+5.5 to +18			1.25	1.0	Down conversion	–	24P	–
MB3889					1.23			–	–	30P
MB39A106		+6.5 to +18						–	–	30P
MB39A116A					1.00			–	–	30P
○MB39A136		+4.5 to +25		1000	0.7			–	–	16P
MB39A104		+7 to +19		1500	1.24			–	24P	–
MB39C011 MB39C011A		+4.5 to +17		2000	1.0			–	–	16P
MB3782	PWM-type controllers for DC/DC converters	+3.6 to +18	3	500	2.5	2.0	Up conversion Down conversion Invert	20P	–	–
MB39A112		+7 to +25		2600	(1.0/ 1.23)	1.0	Down conversion	–	–	20P

○: New product

Packages: P - Plastic

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	Number of Channels	Oscillator frequencies (kHz)	Error amplifiers	Part number	Features
DC/DC converters with switching FET	1	2000/ 3000	Fixed gain type	MB39C014	Current mode type, Synchronous rectification, short circuit protection, Over current detection, Over thermal protection, POWERGOOD
	2	2000	Fixed gain type	MB39C015	Current mode type, Synchronous rectification, short circuit protection, Over current detection, Over thermal protection, Voltage detection circuit
LDO + DC/DC converters with switching FET	2 *	2000	Operational amplifier type	MB39C022G	Current mode type, Synchronous rectification , short circuit protection, Over current protection, Over thermal protection, POWERGOOD, Monitoring of output voltage
					*: 1 ch. is LDO, 1 ch. is DC/DC converter.
DC/DC converters for RF Power Amp.	1	2000	Fixed gain type	MB39C018	Current mode type, Built-in Bypass FET, Synchronous rectification, Output current 800mA (Max.)
DSC/ camcorder DC/DC converters	4	1000	Operational amplifier type	MB3785A	Internal high-precision reference voltage circuit, Channel on/off control function
		1500	Operational amplifier type	MB39A102	Support for control and soft-start of each channel, High-precision reference voltage, Support for external input short detection
				MB39A103	Low voltage operation, Support for control and soft-start of each channel, High-precision reference voltage, Support for external input short detection.
		2000	Operational amplifier type	MB39A110	Synchronous rectification Support for control and soft-start of each channel, High-precision reference voltage, Support for external input short detection
	5	2000	Operational amplifier type	MB39A108	Low voltage operation, Synchronous rectification, Supports for control and soft-start of each channel, High-precision reference voltage, Support for external input short detection
				MB39A115	Synchronous rectification, Supports for control and soft-start of each channel, High-precision reference voltage, Support for external input short detection
	6	800	Operational amplifier type	MB3825A	High-precision reference voltage, Synchronous rectification
		1000	Operational amplifier type	MB3883	Low voltage operation,High-precision reference voltage, Synchronous rectification
		2000	Operational amplifier type	MB39A123	Low voltage operation,Synchronous rectification, Supports for control and soft-start of each channel, High-precision reference voltage, Support for external input short detection
	8	800	Operational amplifier type	MB3881	Low voltage operation, High-precision reference voltage, Synchronous rectification,

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DC/DC converters with switching FET

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage		Output current	Switching FET ON resistance		Solutions	Package	
					(V) (Typ.)	Precision (%)	DC/DC (mA) (Max)	Pch MOS (W) (Typ)	Nch MOS (W) (Typ)		QFN	SON
MB39C014	PWM type DC/DC converters	+2.5 to +5.5	1	2000/3200 (Fix)	1.20	2.0	800	0.3	0.2	Down conversion	–	10P
MB39C015			2	2000 (Fix)	1.30						24P	–

Packages: P - Plastic

DC/DC converters with switching FET + LDO

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz)	Reference voltage (V) (Typ.)	Output voltage (V) (Typ.)	Precision (%)	Output current (mA) (Max.)	Switching FET ON resistance		I/O potential drop (mV) (Typ.)	Solutions	Package
									Pch MOS (Ω) (Typ)	Nch MOS (Ω) (Typ)			SON
◎MB39C022G	DC/DC converter	+2.5 to +5.5	1	2000 (Fix)	0.3	–	±2.5	600	0.3	0.2	–	Down conversion	10P
	LDO		1	–	–	3.3 (Fix)	±2.5	300	–	–	200 (Io = -300mA)		

◎: Now planning

Packages: P - Plastic

DC/DC converters for RF Power Amp.

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage		Output current		Switching FET ON resistance			Solutions	Package
					(V) (Typ.)	Precision (%)	DC/DC (mA) (Max)	Bypass FET (mA) (Max)	Pch MOS (Ω) (Typ)	Nch MOS (Ω) (Typ)	Bypass FET (Ω) (Typ)		QFN
MB39C018	PWM type DC/DC converters Built in Bypass FET	+2.5 to +5.5	1	2000 (Fix)	1.24	1.5	800	1000	0.3	0.2	0.08	Down conversion	24P

Packages: P - Plastic

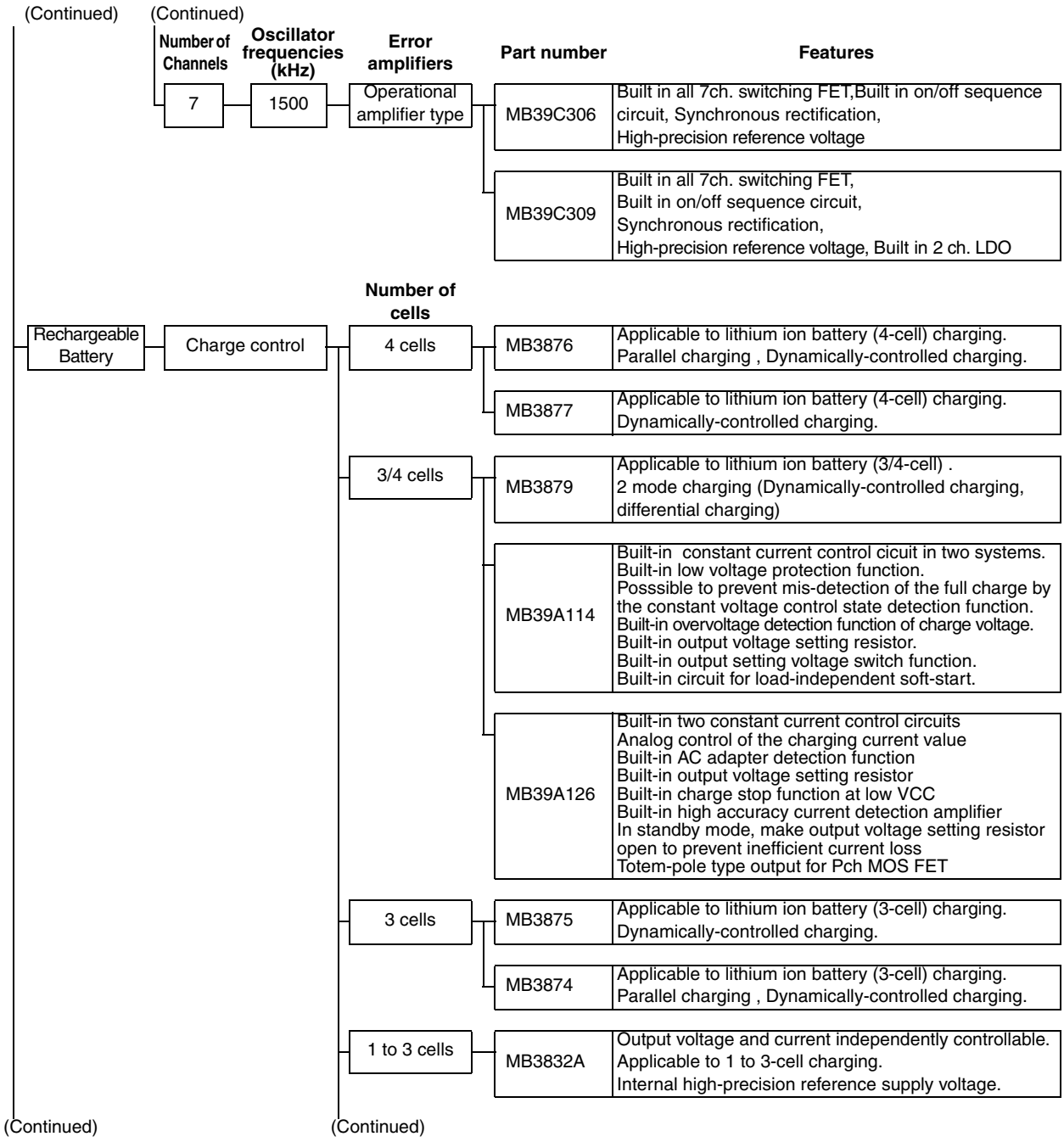
DSC/Camcorder DC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage		Solutions	Drive circuit	Package		
					(V) (Typ.)	Precision (%)			LQFP	BCC	TSSOP
MB3785A	PWM-type controllers for DC/DC converters	+4.5 to +18	4	1000	2.5	1.0	Down conversion	PNP :4	48P	—	—
MB39A102		+2.5 to +11		1500	2.0		Up conversion Down conversion Up/Down conversion	Pch : 3, Nch : 1	—	32P	30P
MB39A103		+1.7 to +11						Pch : 1, Nch : 3	—	32P	30P
MB39A110		+2.5 to +11		2000				Pch : 3, Nch : 1	—	—	38P
MB39A108		+1.7 to +11	5					Pch : 3, Nch : 2	—	40P	38P
MB39A115								Pch : 4, Nch : 1	—	40P	38P
MB3825A		+2.5 to +12	6	800	1.5		Down conversion	PNP : 6	64P**	—	—
MB3883		+1.7 to +9		1000	2.5		Up conversion Down conversion Up/Down conversion	Pch : 2, Nch : 4	48P	48P	—
MB39A123		+1.7 to +11		2000	2.0		Up conversion Down conversion Up/Down conversion Invert	Pch : 4, Nch : 2	48P	48P	—
MB3881		+1.8 to +13	8	800	2.5		Down conversion Up/Down conversion	Pch : 7, Nch : 1	64P*	—	—

*: 0.4 mm pitch **: 0.4 mm pitch, 0.5 mm pitch

Packages: P - Plastic

Power Management Applications



DSC/Camcorder DC/DC Converters

Part number	Function	Power supply voltage (V)	No. of channels	Operating oscillator frequency (kHz) (Max.)	Reference voltage		Solutions	Drive circuit	Package
					(V) (Typ.)	Precision (%)			FBGA
MB39C306	PWM-type DC/DC converters	+2.5 to +6	7	1500	2.4	1.0	Up conversion Down conversion Up/Down conversion Invert	All channel with built-in switching FETs	103P
MB39C309		+2.5 to +5.5	7 (DC/DC) 2 (LDO						82P

Packages: P - Plastic

Rechargeable Battery (Charge control)

Part number	Function	Power supply voltage (V)	Output voltage (V)	Precision (%)		Number of cells	Operating oscillator frequency (kHz) (Max.)	Solutions	Package		
				Ta = +25 °C	Ta = -30 to +85 °C				SSOP	LQFP	QFN
MB3876	Charge control DC/DC converters	+7 to +25	16.8	±0.8	±1.0	4	500	Down conversion	24P	–	–
MB3877									24P	–	–
MB3879		+8 to +25	12.6/16.8	±0.8	±1.0	3/4			—	48P	—
			12.3/16.4	±0.9	±1.1						
MB39A114			12.6/16.8	±0.5	±0.74 *				24P	–	–
MB39A126				±0.6	±0.80 *				24P	–	28P
MB3875		+7 to +25	12.6	±0.8	±1.0	3			24P	–	–
MB3874									24P	–	–
MB3832A		+3.6 to +18	Any voltage level	±0.5	±1.0*	1 to 3			20P	–	–

* : Ta = -10 to +85 °C

Package: P-plastic

Power Management Applications

(Continued)

(Continued)

Number of cells	Part number	Features
1 to 4 cells	MB3878	Output voltage and current are independently controllable. Applicable to 1 to 4-cell charging. Internal high-precision reference supply voltage, Dynamically-controlled charging.
	MB3887	Output voltage and current are independently controllable. Applicable to 1 to 4-cell charging. Internal high-precision reference supply voltage. High charging current accuracy. Dynamically-controlled charging.
	MB3888	Output voltage and current are independently controllable. Applicable to 1 to 4-cell charging. Internal high-precision reference supply voltage. High charging current accuracy.
	MB39A113	Built-in constant current control cicuit in two systems. Built-in low voltgae protection function. Posssible to prevent mis-detection of the full charge by the constant voltage control state detection function. Built-in overvoltage detection function of charge voltage. Built-in circuit for load-independent soft-start.
	MB39A118	Built-in off time control function, Built-in constant current control circuit in two systems, Possible to control of the constant current by analog value, Built-in for Nch MOS FET synchronous rectification type output stage, Built-in battery select function, Possible to set any output voltage by external resistor, In IC standby mode, leave output voltage setting resistor open to prevent inefficient current loss
	MB39A119	Built-in off time control function, Built-in voltage detection function of AC adapter, Possible to prevent mis-detection of the full charge by the constant voltage control state detection function, Built-in constant current control circuit in two systems, Possible to control of the constant current by analog value, Built-in for Nch MOS FET synchronous rectification type output stage, Built-in charge stop function at low VCC, Possible to set any output voltage by external resistor, In IC standby mode, leave output voltage setting resistor open to prevent inefficient current loss
	MB39A125	Built-in two constant current control circuits, Analog control of the charging current value, Built-in AC adapter detection function, External output voltage setting resistor, Built-in charge stop function at low VCC, Built-in high accuracy current detection amplifier, In standby mode, make output voltage setting resistor open to prevent inefficient current loss, Totem-pole type output for Pch MOS FET
2 to 4 cells	MB39A129	Built-in two constant current control loops, Built-in AC adapter detection function (ACOK terminal), Built-in output voltage control setting without external resistor, Adjustable output voltage with external resistor, Built-in two high accuracy current detection amplifiers, Built-in Charging Current Control setting without resistor, Adjustable charging current with external resistor, Support for frequency setting using an external resistor, (Frequency setting capacitor integrated), Built-in under voltage lockout protection, In standby mode, only AC adapter detection function is operated, Built-in VH regulator for reducing Qg loss of Pch MOS FET
	MB39A134	Built-in two constant current control loops, Built-in AC adapter detection function (ACOK terminal), Built-in output voltage control setting without external resistor, Adjustable output voltage with external resistor, Built-in two high accuracy current detection amplifiers, Built-in Charging Current Control setting without resistor, Adjustable charging current with external resistor, Support for frequency setting using an external resistor, (Frequency setting capacitor integrated), Built-in under voltage lockout protection, In standby mode, only AC adapter detection function is operated, Built-in VH regulator for reducing Qg loss of P-ch MOS FET

	Number of channels	Topology		
DC/DC converters for UMPC	6	Current Mode	MB39C308	For LPIA Platform VR, N/N Synchronous rectification, Integrated FET Driver for external MOSFETs(2ch), Integrated Switching MOSFETs(4ch), Preset Output Voltage, Soft start function/Soft stop function, Power good function, Various protection circuitry(SCP/OTP/OVP/OCP/UVLO/IVP)

(Continued)

Rechargeable Battery (Charge control)

Part number	Function	Power supply voltage (V)	Output voltage (V)	Precision (%)		Number of cells	Operating oscillator frequency (kHz) (Max.)	Solutions	Package		
				Ta = +25 °C	Ta = -30 to +85 °C				SSOP	TSSOP	QFN
MB3878	Charge control DC/DC converters	+7 to +25	4.2 V/cell	±0.8	±1.0	1 to 4	500	Down conversion	24P	–	–
MB3887		+8 to +25		+0.6 -0.4	±0.74 *				24P	–	–
MB3888			Any voltage level	±0.5					20P	–	–
MB39A113			4.2 V/cell						24P	–	–
MB39A118					±0.74 *		1000		–	–	28P
MB39A119									–	–	28P
MB39A125							500		24P	–	28P
MB39A129			4.145V/Cell, 3.75V/Cell, Any voltage level		±0.7 *	2 to 4	2000		24P	–	–
○MB39A134			4.2V/Cell, 4.1V/Cell, Any voltage level	±0.5	±0.7 *	2 to 4	2000		–	24P	–

* : Ta = -10 to +85 °C
Package: P-plastic
○: New product

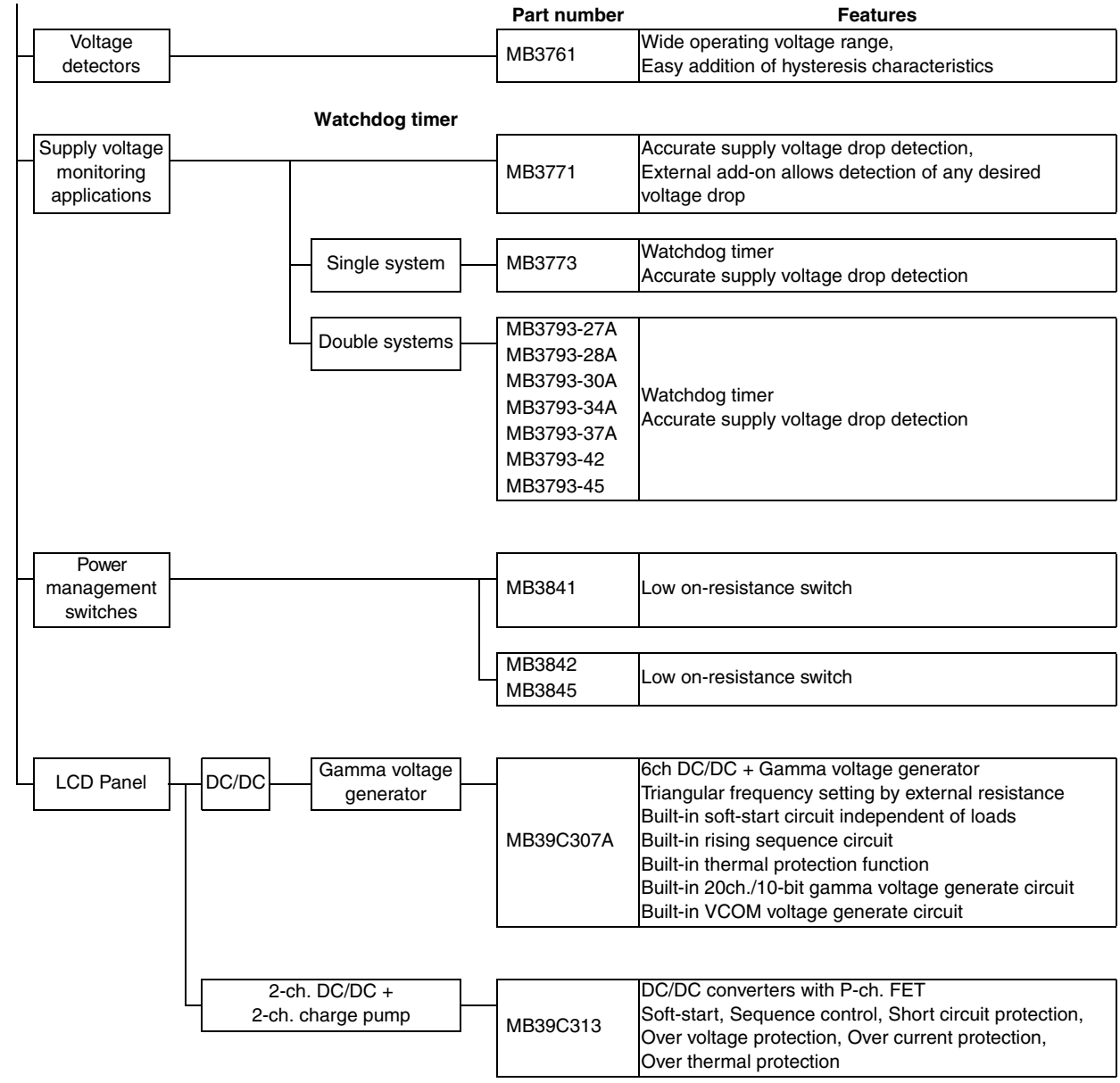
DC/DC converters for Ultra Mobile PC

Part number	Function	Input voltage (V)	Number of channels	Oscillator frequencies (kHz)	Output features				Solutions	Package
					Pin name	Preset Output Voltage (V)	FET	Drive or Output current (A) (Max)		PBGA
○MB39C308	DC/DC converters for LPIA Platform VR	+5.5 to +12.6	6	700 (Fix)	CH1	5	External	2	Down conversion	208P
					CH2	3.3		4.5		
					CH3	1.8/1.5	Integrated	2.7		
					CH4	0.9/0.75		1.5		
					CH5	1.5		2.5		
					CH6	1.05		3.5		

LPIA=Low Power Intel Architecture®
Package: P-plastic
○: New product

Power Management Applications

(Continued)



Voltage Detectors

Part number	Function	Power supply voltage (V)	Reference voltage (V) (Typ.)	Package
				SOP
MB3761	Voltage detector	+2.5 to +40	1.2	8P

Package: P - Plastic

Supply Voltage Monitoring Applications

Part number	Function	Power supply voltage (V)	Detection voltage (V)	Reset certified voltage (V) (Typ.)	Package	
					SOP	SSOP
MB3771	Supply voltage monitoring applications	+3.5 to +18	Any voltage level in addition to 4.2 V	0.8	8P	–
MB3773	Supply voltage monitoring applications with watchdog timer	+3.5 to +16			8P	–
MB3793-27A *1	Supply voltage monitoring applications with dual watchdog timer systems	+4 (Max.)	2.7±0.07		8P	8P
MB3793-28A *1			2.8±0.07		8P	8P
MB3793-30A *1		+6 (Max.)	3.0±0.07		8P	8P
MB3793-34A *1			3.4±0.08		8P	(8P)*2
MB3793-37A *1			3.7±0.1		8P	(8P)*2
MB3793-42 *1			4.2±0.1		8P	(8P)*2
MB3793-45 *1			4.5±0.1		8P	8P

*1:Detection voltages of the MB3793 series are available in the range from 2.4 V to 4.9 V in 0.1 V increments. Consult with supplier. Package: P - Plastic

*2:( ) option

Switching Applications

Part number	Function	Power supply voltage (V) (Max.)	Number of channels	On-resistance (Ω)	Drive current (A) (Max.)	Package	
						SOP	SSOP
MB3841	Power management switch	5.5	1	0.045	2.0	8P	–
MB3842			2	0.1	0.6	–	20P
MB3845							

Package: P - Plastic

LCD Panel

Part number	Function	DC/DC Block						Gamma volrtage generator block			Package
		Power supply voltage (V)	Number of channels	Reference voltage (V)	Precision (%)	Oscillation frequency (kHz)(Max)	Solution	Gamma voltage number of channel	VCOM voltage number of channel	DAC (bit)	BCC
○MB39C307A	DC/DC + Gamma voltage generator	+4.5 to +17	6	1 1.25	± 1.0	600	Step down 3ch Step up 2ch Invert 1ch	20	1	10	92P *

○: New product

*: With exposed pad

Package: P - Plastic

LCD Panel

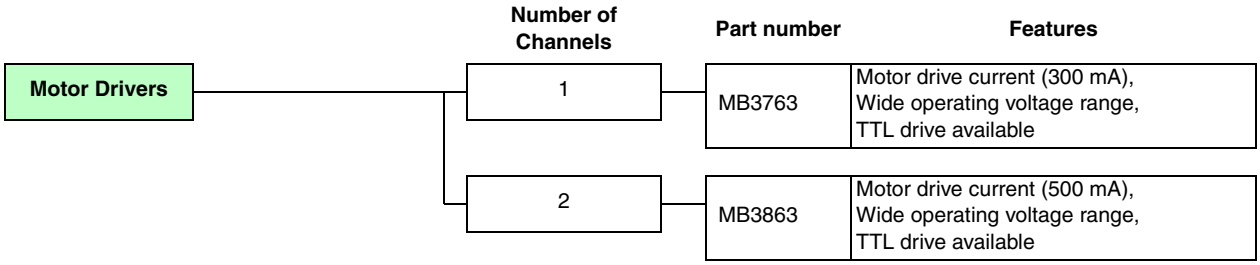
Part number	Function	Power supply voltage (V)	Number of channels	Reference voltage (V)	Precision	Oscillation frequency (kHz)	Solution	Package
								TSSOP
◎MB39C313	2ch. DC/DC + 2ch. charge pump	+8 to +14	4	1.213	± 1.0%	500/750	Step down	28P *
				1.146	± 1.0%		Step up	
				0	± 36mV		Invert charge pump	
				1.213	± 1.0%		Step up charge pump	

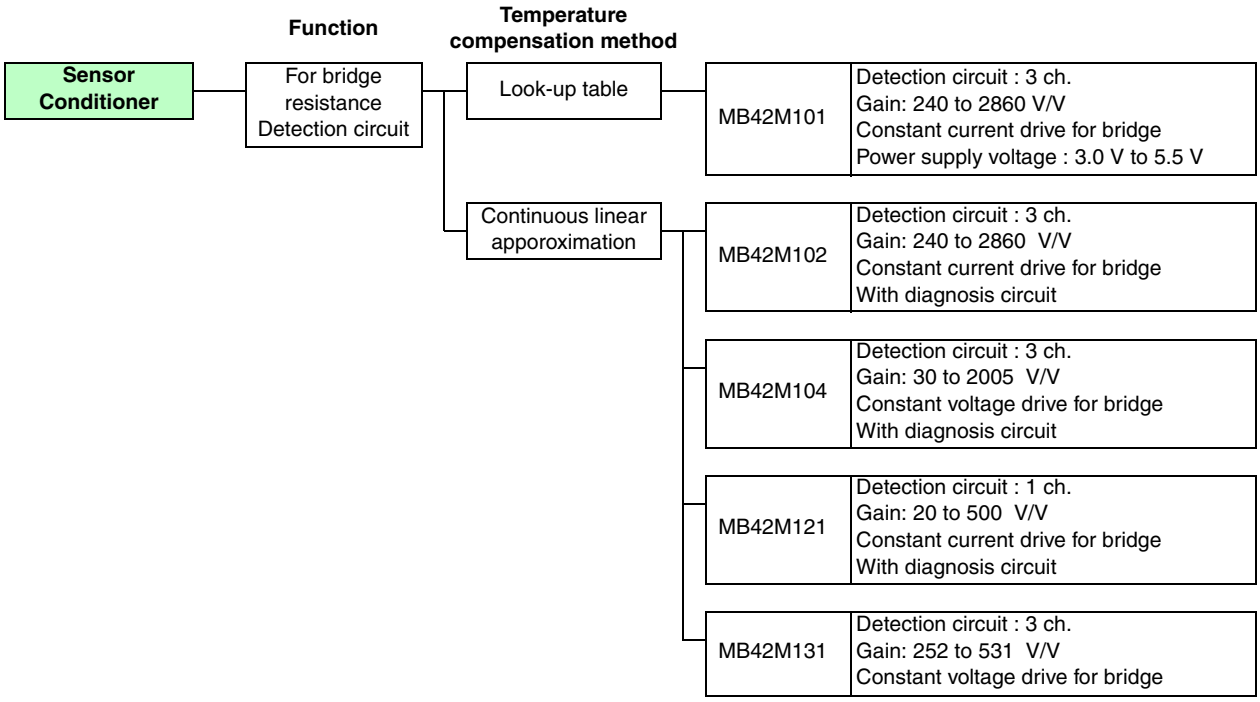
◎: Now planning

*: With exposed pad

Package: P - Plastic

Motor Drivers/Sensor Conditioner





Motor Drivers

Part number	Function	Number of Channels	Output current (mA)	Power supply voltage (V)	Package
					SOP
MB3763	Reversible motor drivers	1	300	+4 to +18	8P
MB3863		2	500	+4 to +36	20P

Package: P - Plastic

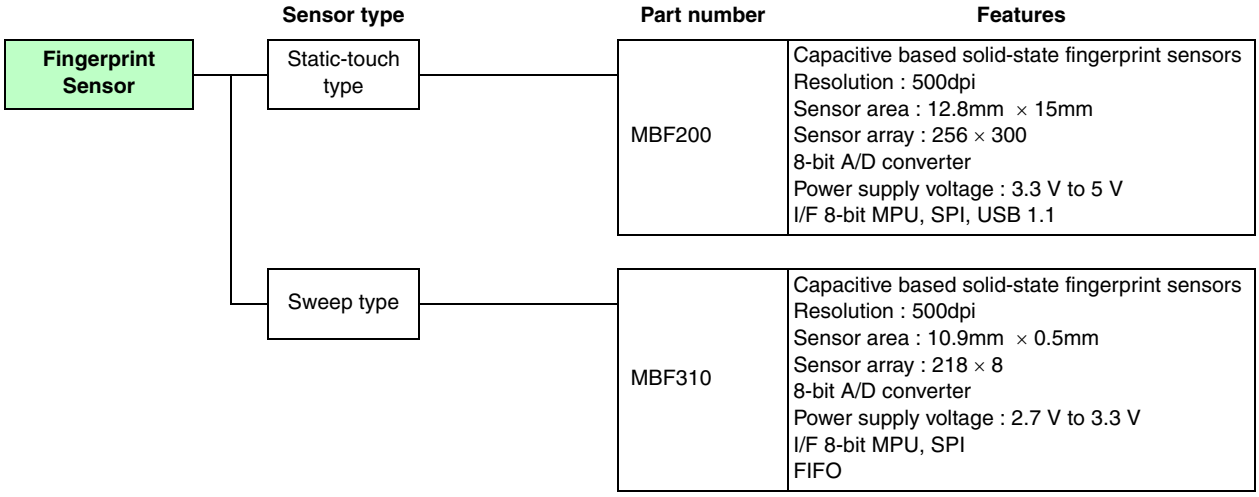
Sensor Conditioner

Part number	Function	Temperature compensation method	Number of detection circuits	Gain	Power supply voltage (V)	Others	Package	
							BCC	SSOP
MB42M101	For bridge resistance Detection circuit	Look-up table	3	240 to 2860 V/V	3.0 to 5.5	Digital compensation Constant current drive Built-in memory 1280 bits	32P	–
MB42M102	For bridge resistance Detection circuit	Continuous linear apporoximation	3	240 to 2860 V/V	4.5 to 5.5	Digital compensation Constant current drive Built-in memory 1280 bits Diagnosis circuit	40P	–
MB42M104	For bridge resistance Detection circuit	Continuous linear apporoximation	3	30 to 2005 V/V	4.5 to 5.5	Digital compensation Constant voltage drive Built-in memory 1280 bits Diagnosis circuit	40P	–
◎MB42M121	For bridge resistance Detection circuit	Continuous linear apporoximation	1	20 to 500 V/V	2.7 to 3.6	Digital compensation Constant voltage drive Built-in memory 1280 bits Diagnosis circuit	–	20P
◎MB42M131	For bridge resistance Detection circuit	Continuous linear apporoximation	3	252 to 531 V/V	2.7 to 3.6	Digital compensation Constant voltage drive	20P	–

◎: Now planning

Package: P - Plastic

Fingerprint Sensor

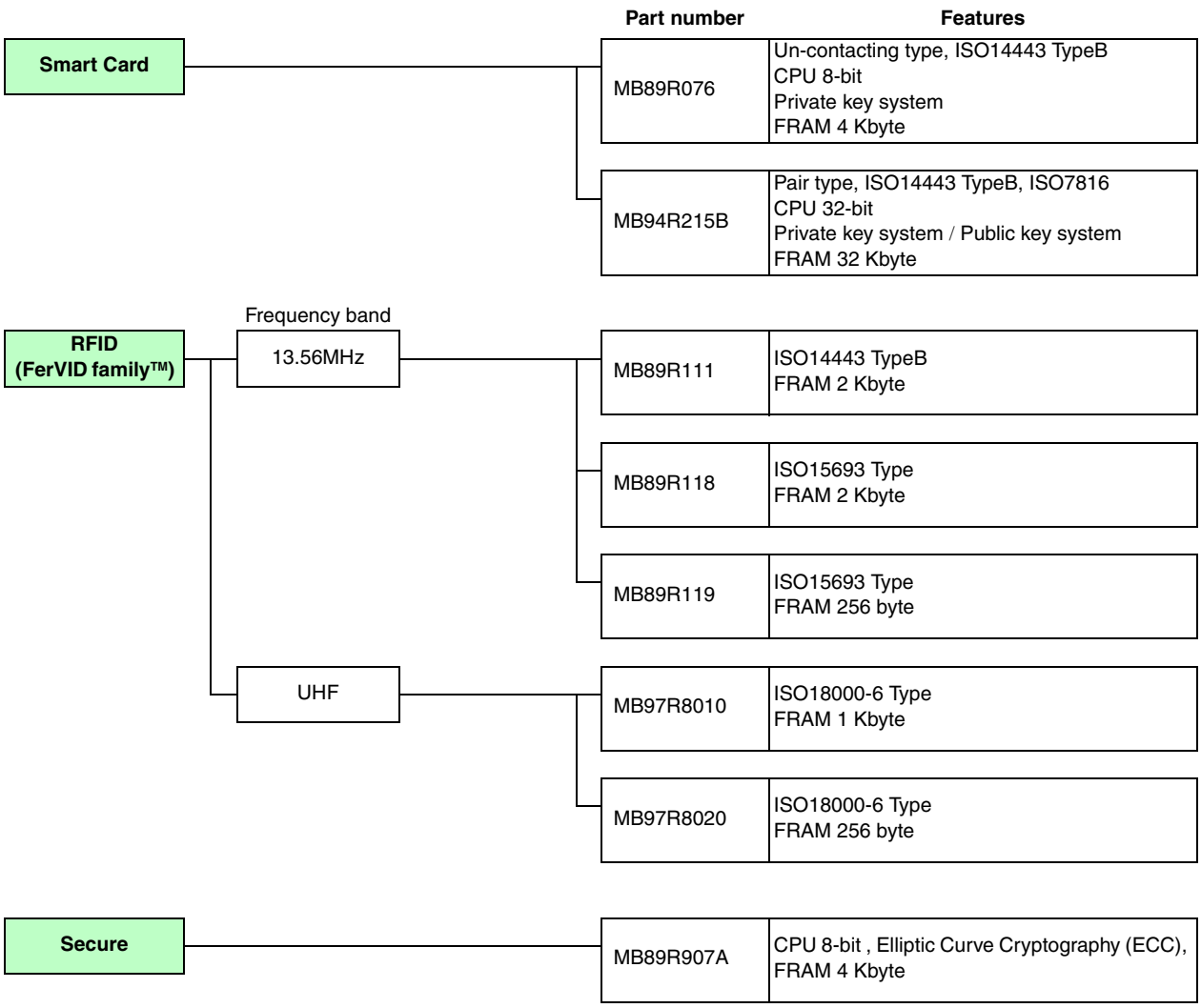


Fingerprint Sensor

Part number	Resolution (dpi)	Sensor area (mm)	Sensor array (pixel)	Power supply voltage (V)	Interface	Others	Package	
							TSOP	FBGA
MBF200	500	12.8 × 15.0	256 × 300	3.3 to 5.0	8bit MPU SPI USB 1.1	-	80P	-
MBF310		10.9 × 0.5	218 × 8	2.7 to 3.3	8bit MPU SPI	FIFO	-	43P

Package: P - Plastic

Smart Card/RFID (FerVID family™) /Secure



Smart Card/RFID (FerVID family™) /Secure

Smart Card

Part number	Interface	CPU (bit)	FRAM (byte)	ROM (byte)	SRAM (byte)	Code Type	Shipment form
MB89R076	ISO14443 TypeB	8	4K	32K	512	DES	An exclusive package
MB94R215B	ISO14443 TypeB, ISO7816	32	32K	128K	8K	DES/RSA	An exclusive package

RFID (FerVID family™)

Part number	Frequency band	Interface	Transmission speed (Reader/Writer -> LSI)	Transmission speed (LSI -> Reader/Writer)	FRAM (byte)	Shipment form
MB89R111	13.56MHz	ISO14443 TypeB	106kbps, 212kbps	106kbps, 212kbps	2K	Wafer
MB89R118		ISO15693	26.48kbps (52.97kbps)	26.48kbps (52.97kbps)	2K	Wafer (With a golden Bump)
MB89R119		ISO15693	26.48kbps (52.97kbps)	26.48kbps (52.97kbps)	256	Wafer (With a golden Bump)
○MB97R8010	UHF	ISO18000-6 TypeB	10kbps, 40kbps	10kbps, 40kbps	1K	Wafer (With a golden Bump)
○MB97R8020		ISO18000-6 TypeB	10kbps, 40kbps	10kbps, 40kbps	256	Wafer (With a golden Bump)

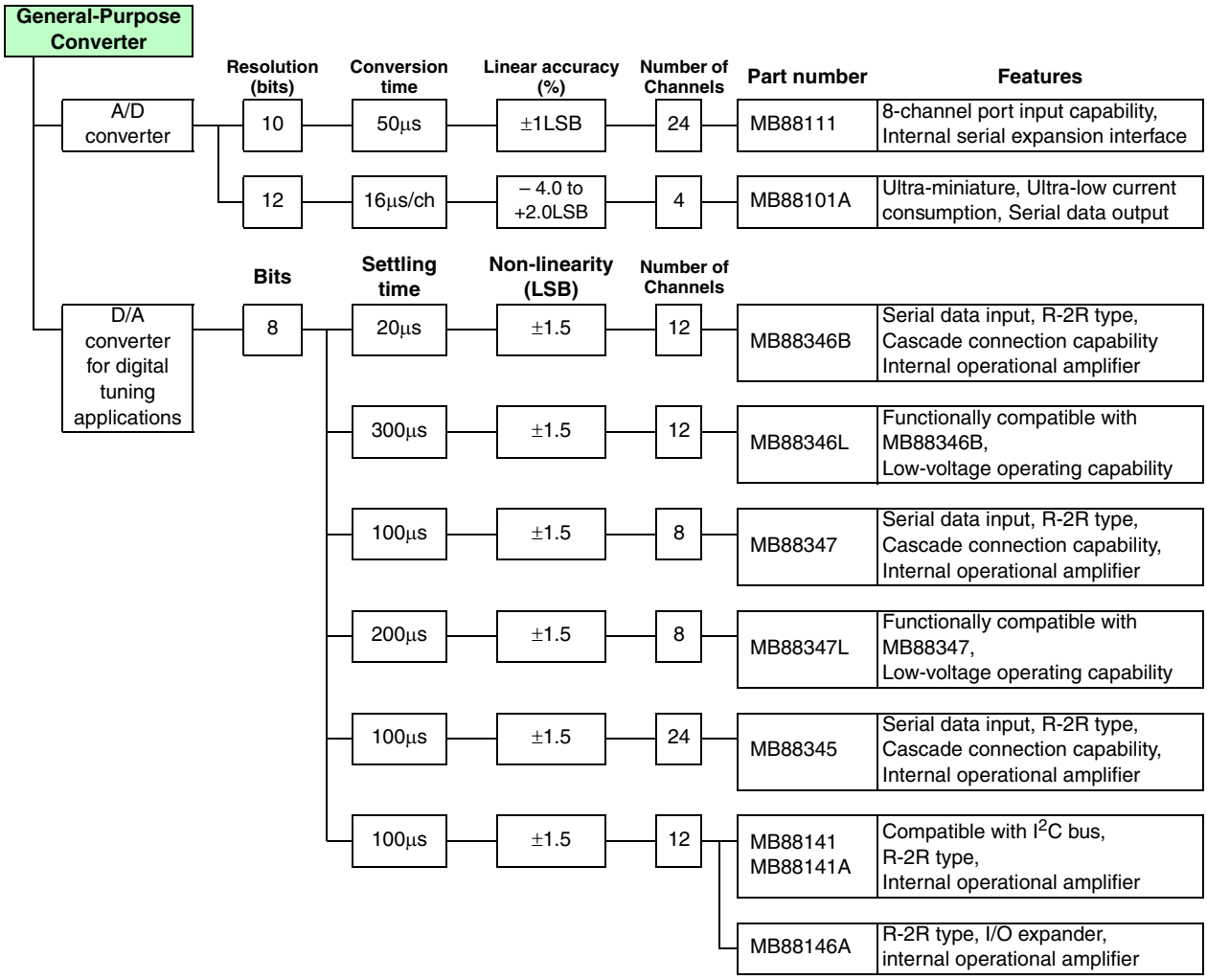
○: New product

Secure

Part number	CPU (bit)	FRAM (byte)	ROM (byte)	SRAM (byte)	Code Type	Power supply voltage (V)	Package
							QFP
MB89R907A	8	4K	32K	1K	Elliptic Curve Cryptography (ECC)	+5 ± 5%	48P

Package: P - Plastic

General-Purpose Converter



General-Purpose Converter

A/D Converter

Part number	Function	Conversion method	Conversion time (µs/ch) (Max.)	Linearity error (%) (Max.)	Power supply voltage (V)	Package				
						DIP	SOP	SSOP	QFP	SH-DIP
MB88111	24-ch 10-bit A/D converter	Successive approximation	50	±1 LSB	+3.5 to +5.5	–	–	–	44P	48P
MB88101A	4-ch 12-bit A/D converter		16 (at 5 V±10%)	-4.0 to +2.0 LSB	+3.3 to +5.5	16P	16P	16P	–	–

Packages: P - Plastic

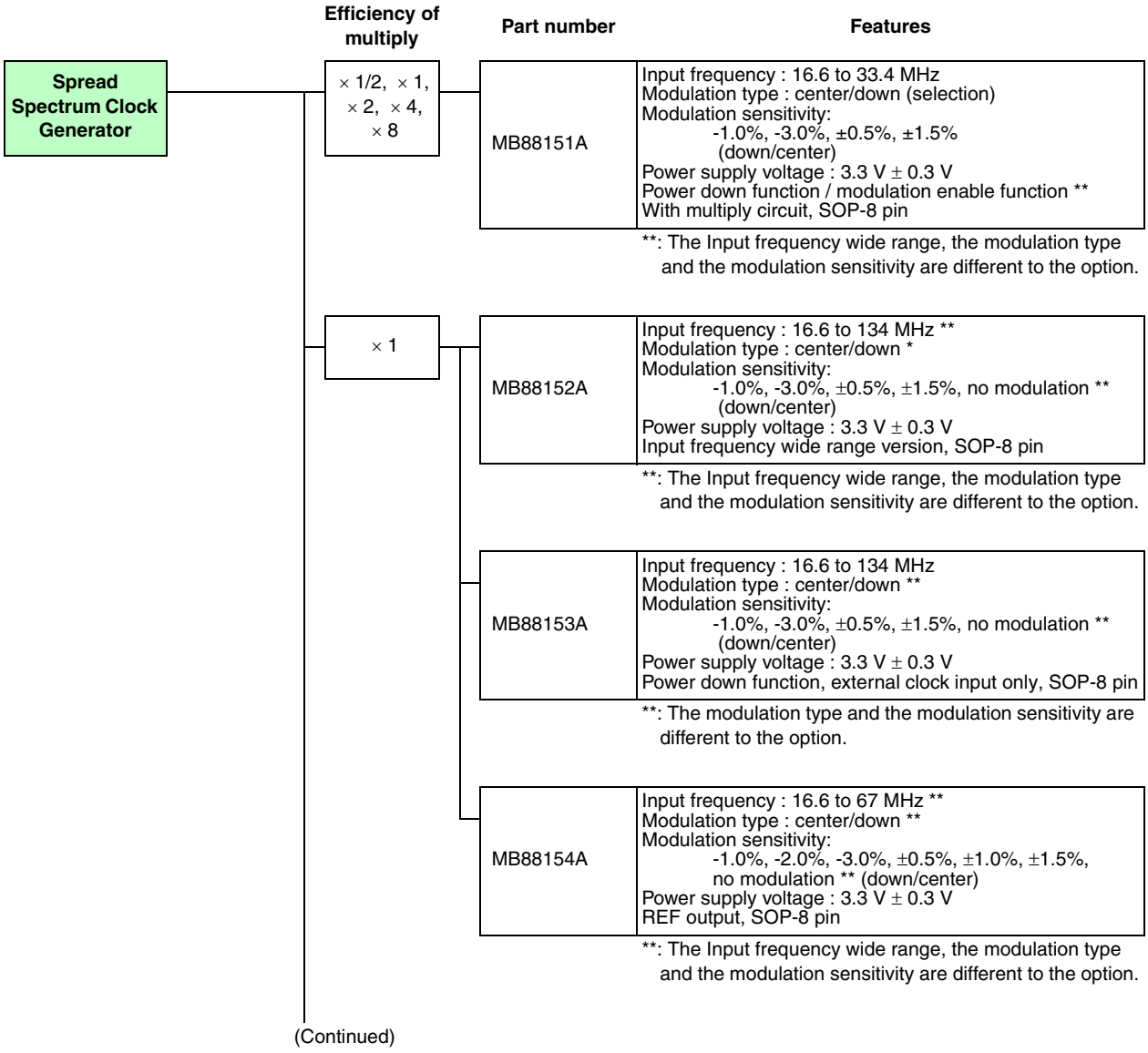
D/A Converter for Digital Tuning Applications

Part number	Function	Settling time (µs) (Max.)	Power consumption (mW) (Typ.)	Non-linearity error (LSB)	Power supply voltage (V)	Package			
						DIP	SOP	SSOP	QFP
MB88346B	12-ch 8-bit D/A converter (internal operational amplifier)	20	14	±1.5	+5±10%	20P	20P	20P	–
MB88346L	12-ch 8-bit D/A converter (internal operational amplifier, low voltage operation)	300	5		+2.7 to +3.6	20P	20P	20P	–
MB88347	8-ch 8-bit D/A converter (internal operational amplifier)	100	9		+5±10%	16P	16P	16P	–
MB88347L	8-ch 8-bit D/A converter (internal operational amplifier, low voltage operation)	200	4.2		+2.7 to +3.6	16P	16P	16P	–
MB88345	24-ch 8-bit D/A converter (internal operational amplifier)	100	27		+5±10%	–	–	–	32P
MB88141 *	12-ch 8-bit D/A converter (compatible with I²C bus, internal operational amplifier)	100	15			24P	24P	24P	–
MB88141A *									–
MB88146A	12-ch 8-bit D/A converter (I/O expander, internal operational amplifier)		14.5		Digital:+2.7 to +5.5 Analog:+5±10%	24P	–	24P	–

Package: P - Plastic

* “Purchase of Fujitsu Microelectronics I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.”

Spread Spectrum Clock Generator



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Spread Spectrum Clock Generator

Part number	Function	Power supply voltage	Input frequency (MHz)	Efficiency of multiply	Output frequency (MHz)	Modulation Type	Modulation sensitivity	Other	Package
									SOP
MB88151A-100	EMI noise reduction PLL (SSCG)	3.3 ± 0.3	16.6 to 33.4	× 1	16.6 to 33.4	Down or center (selection)	-1.0%, -3.0% (down) ±0.5%, ±1.5% (center) no modulation (no modulation setting is no PD product)	PD function disable	8P
MB88151A-101								PD function enable	
MB88151A-200				× 2	33.2 to 66.8			PD function disable	
MB88151A-201								PD function enable	
MB88151A-400				× 4	66.4 to 133.6			PD function disable	
MB88151A-401								PD function enable	
MB88151A-500				× 1/2	8.3 to 16.7			PD function disable	
MB88151A-501								PD function enable	
MB88151A-800			8.3 to 16.7	× 8	66.4 to 133.6			PD function disable	
MB88151A-801								PD function enable	
MB88152A-100			16.6 to 40 33 to 67 40 to 80 66 to 134	× 1	16.6 to 40 33 to 67 40 to 80 66 to 134	Down	-1.0%, -3.0%	-	8P
MB88152A-110						Center	±0.5%, ±1.5%		
MB88152A-101			16.6 to 40 33 to 67		16.6 to 40 33 to 67	Down	-1.0%, -3.0% no modulation		
MB88152A-111						Center	±0.5%, ±1.5% no modulation		
MB88152A-102			40 to 80 66 to 134		40 to 80 66 to 134	Down	-1.0%, -3.0% no modulation		
MB88152A-112						Center	±0.5%, ±1.5% no modulation		
MB88153A-100			16.6 to 40 66 to 134 33 to 67 40 to 80	× 1	16.6 to 40 66 to 134 33 to 67 40 to 80	Down	-1.0%, no modulation	PD function enable	8P
MB88153A-101							-3.0%, no modulation		
MB88153A-110						Center	±0.5%, no modulation		
MB88153A-111							±1.5%, no modulation		
MB88154A-102			33 to 67	× 1	33 to 67	Down	-1.0%, -2.0%, 3.0%, no modulation	REF output enable	8P
MB88154A-103			16.6 to 40		16.6 to 40				
MB88154A-112			33 to 67		33 to 67	Center	±0.5%, ±1.0%, ±1.5%, no modulation		
MB88154A-113			16.6 to 40		16.6 to 40				

Package: P - Plastic

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Efficiency of multiply	Part number	Features
× 1, × 4	MB88155	Input frequency : 12.5 to 50 MHz (× 1) * 12.5 to 20 MHz (× 4) Modulation type : center/down * Modulation sensitivity: -1.0%, -2.0%, ±0.5%, ±1.0%, no modulation * (down/center) Power supply voltage : 3.3 V ± 0.3 V Power down function / modulation enable function TSSOP-8 pin
		*: The Input frequency wide range, the modulation type and the modulation sensitivity are different to the option.
× 1, × 2, × 4 (selection)	MB88156	Input frequency : 12.5 to 50 MHz Modulation type : center/down (selection) Modulation sensitivity: -1.0%, -2.0%, -3.0%, ±0.5%, ±1.5%, no modulation (down/center) Power supply voltage : 3.3 V ± 0.3 V REF output/none With multiply circuit, BCC-16 pin
× 1, × 2, (selection)	MB88161	Input frequency : 20 to 28 MHz Modulation type : center/down (selection) Modulation sensitivity: -1.0%, -2.0%, -4.0%, ±0.5%, ±1.0%, ±2.0%, no modulation (down/center) Power supply voltage : 3.3 V ± 0.3 V Power down function, BCC-18 pin
× 1, × 4, (selection)	MB88162	Input frequency : 12 to 28 MHz Modulation type : center/down (selection) Modulation sensitivity: -1.0%, -2.0%, -4.0%, ±0.5%, ±1.0%, ±2.0%, no modulation (down/center) Power supply voltage : 3.3 V ± 0.3 V Power down function, BCC-18 pin
× 1, × 2, × 4	MB88163 (Under development)	Input frequency : 12.5 to 42 MHz * Modulation type : center Modulation sensitivity: ±0.25%, ±0.5%, ±1.0%, no modulation (center) Power supply voltage : 1.8 V ± 0.15 V Output enable function * TSSOP-8 pin/BCC-6 pin
		*: The Input frequency wide range, modulation sensitivity and output enable function are different to the option.
× 1/2 or more (MASK option)	MB88181	Input frequency : 16 to 32 MHz Modulation type : center Modulation sensitivity: ±0.5%, ±1.0%, ±1.5%, ±2.0%, no modulation (center) Power supply voltage : 3.3 V ± 0.3 V Clock output 8(Max.), power down function, TSSOP-20 pin
		*: The efficiency of multiply and the output mode can be arbitrarily set by the mask option.

(Continued)

Part number	Function	Power supply voltage (V)	Input frequency (MHz)	Efficiency of multiply	Output frequency (MHz)	Modulation Type	Modulation sensitivity	Other	Package	
									TSSOP	BCC
MB88155-100	EMI noise reduction PLL (SSCG)	3.3 ± 0.3	12.5 to 25	× 1	12.5 to 25	Down	-1.0%, -2.0% no modulation	PD function disable	8P	-
MB88155-101			25 to 50		25 to 50					
MB88155-102			12.5 to 25		12.5 to 25		-1.0%, -2.0%	PD function enable		
MB88155-103			25 to 50		25 to 50					
MB88155-110			12.5 to 25		12.5 to 25	Center	±0.5%, ±1.0% no modulation	PD function disable		
MB88155-111			25 to 50		25 to 50					
MB88155-112			12.5 to 25		12.5 to 25		±0.5%, ±1.0%	PD function enable		
MB88155-113			25 to 50		25 to 50					
MB88155-400			12.5 to 20	× 4	50 to 80	Down	-1.0%, -2.0% no modulation	PD function disable		
MB88155-402							-1.0%, -2.0%	PD function enable		
MB88155-410						Center	±0.5%, ±1.0% no modulation	PD function disable		
MB88155-412							±0.5%, ±1.0%	PD function enable		
MB88156-000			20 to 28 (× 1) 14 to 40 (× 2)	× 1, × 2, (selection)	20 to 28 (× 1) 28 to 80 (× 2)	Down/ Center (selection)	-1.0%, -2.0%, ±0.5%, ±1.0%, no modulation	REF output enable	-	16P
MB88156-001								REF output disable		
MB88161			12 to 28 (× 1) 20 to 42 (× 4)	× 1, × 4 , (selection)	12 to 28 (× 1) 80 to 168 (× 4)		-1.0%, -2.0%, -4.0%, ±0.5%, ±1.0%, ±2.0%, no modulation	PD function enable	-	18P
MB88162			12 to 28 (× 1) 20 to 42 (× 4)	× 1, × 4 , (selectable)	12 to 28 (× 1) 80 to 168 (× 4)	Down/ Center (selectable)	-1.0%, -2.0%, -4.0%, ±0.5%, ±1.0%, ±2.0%, no modulation	PD function enable	-	18P
◎ MB88163		1.8 ± 0.15	12.5 to 26	× 1	12.5 to 26	Center	±0.5%, no modulation	-	-	6P
◎ MB88163-100			20 to 42		20 to 42		±0.25%, ±0.5%, ±1.0%, no modulation	OE function enable	8P	-
◎ MB88163-200				× 2	40 to 84					
◎ MB88163-400				× 4	80 to 168					
◎ MB88163-500			12.5 to 26	× 1	12.5 to 26					
MB88181		3.3 ± 0.3	16 to 32	× 1/2 or more *	8 to 166	Center	±0.5%, ±1.0%, ±1.5%, ±2.0%, no modulation	PD function enable, Clock output 8(Max.)	20P	-

*: The efficiency of multiply and the output mode can be arbitrarily set by the mask option. Package: P - Plastic

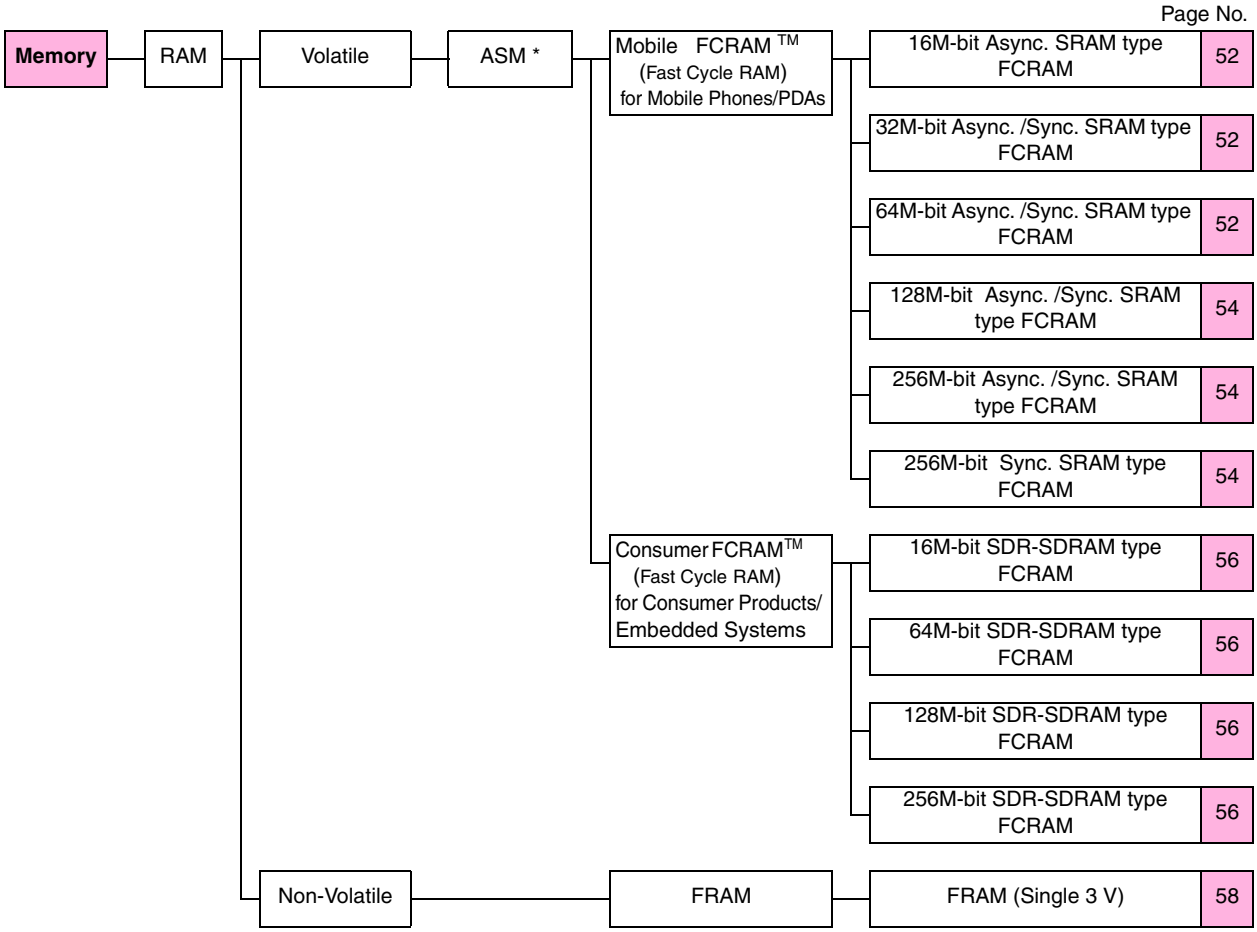
◎: Now planning

SSCG Simple Evaluation Board

Part number		Remarks	
MB88151A	MB88151AEB01-100	MB88151A-100 mounted	An oscillation vibrator, oscillation stable capacity, and a power supply line are required.
	MB88151AEB01-101	MB88151A-101 mounted	
	MB88151AEB01-200	MB88151A-200 mounted	
	MB88151AEB01-201	MB88151A-201 mounted	
	MB88151AEB01-400	MB88151A-400 mounted	
	MB88151AEB01-401	MB88151A-401 mounted	
	MB88151AEB01-500	MB88151A-500 mounted	
	MB88151AEB01-501	MB88151A-501 mounted	
	MB88151AEB01-800	MB88151A-800 mounted	
	MB88151AEB01-801	MB88151A-801 mounted	
MB88152A	MB88152AEB01-100	MB88152A-100 mounted	
	MB88152AEB01-110	MB88152A-110 mounted	
	MB88152AEB01-101	MB88152A-101 mounted	
	MB88152AEB01-111	MB88152A-111 mounted	
	MB88152AEB01-102	MB88152A-102 mounted	
	MB88152AEB01-112	MB88152A-112 mounted	
MB88153A	MB88153AEB01-100	MB88153A-100 mounted	
	MB88153AEB01-101	MB88153A-101 mounted	
	MB88153AEB01-110	MB88153A-110 mounted	
	MB88153AEB01-111	MB88153A-111 mounted	
MB88154A	MB88154AEB01-102	MB88154A-102 mounted	
	MB88154AEB01-103	MB88154A-103 mounted	
	MB88154AEB01-112	MB88154A-112 mounted	
	MB88154AEB01-113	MB88154A-113 mounted	
MB88155	MB88155EB01-100	MB88155-100 mounted	
	MB88155EB01-101	MB88155-101 mounted	
	MB88155EB01-102	MB88155-102 mounted	
	MB88155EB01-103	MB88155-103 mounted	
	MB88155EB01-110	MB88155-110 mounted	
	MB88155EB01-111	MB88155-111 mounted	
	MB88155EB01-112	MB88155-112 mounted	
	MB88155EB01-113	MB88155-113 mounted	
	MB88155EB01-400	MB88155-400 mounted	
	MB88155EB01-402	MB88155-402 mounted	
	MB88155EB01-410	MB88155-410 mounted	
	MB88155EB01-412	MB88155-412 mounted	
MB88156	MB88156EB01-BC16-000	MB88156-000 mounted	
	MB88156EB01-BC16-001	MB88156-001 mounted	
MB88161	MB88161EB01	MB88161 mounted	
MB88162	MB88162EB01	MB88162 mounted	
MB88163	◎MB88163EB01	MB88163 mounted	
	◎MB88163EB01	MB88163-100 mounted	
	◎MB88163-200EB02	MB88163-200 mounted	
	◎MB88163-400EB02	MB88163-400 mounted	
	◎MB88163-500EB02	MB88163-500 mounted	

◎: Now planning

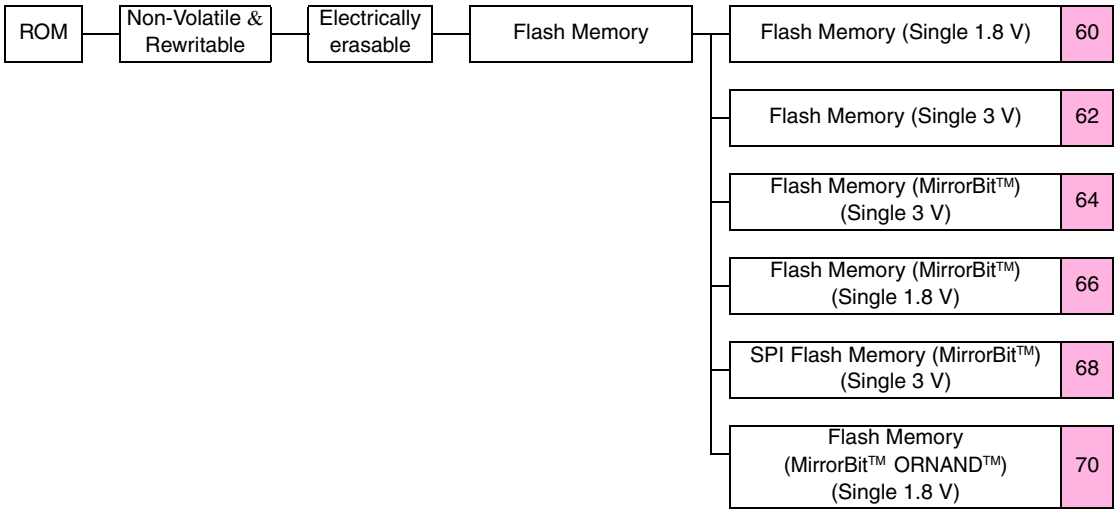
Memory Product Line-up



* : ASM =Application Specific Memory

FCRAM is a trademark of Fujitsu Microelectronics Limited.

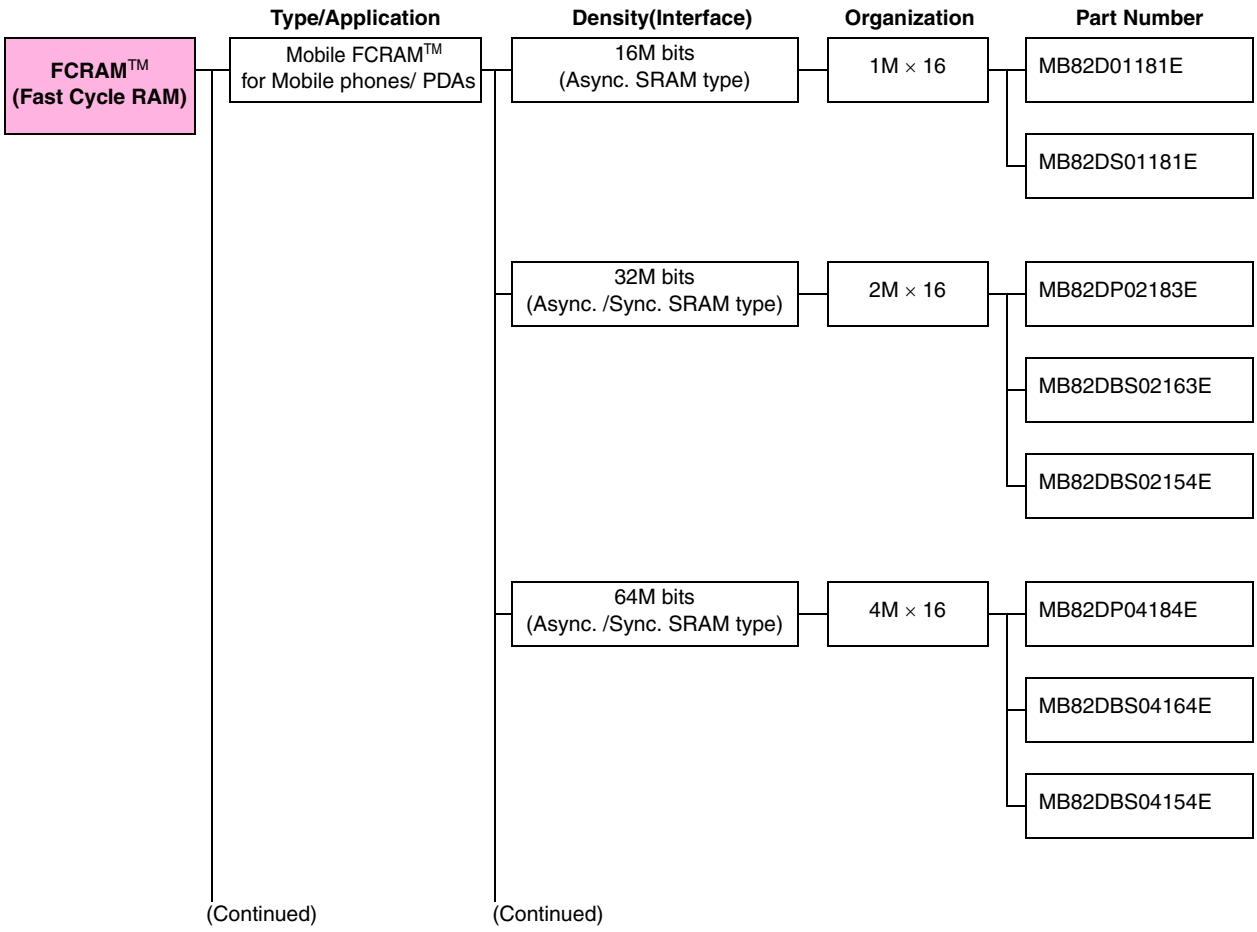
SPANSION™ Products



MirrorBit is a trademark of Spansion Inc.

ORNAND is a trademark of Spansion Inc.

FCRAM™ (Fast Cycle RAM) (1)



FCRAM is a trademark of Fujitsu Microelectronics Limited.

Mobile FCRAM™ (Fast Cycle RAM)

• 16M-bit Async. SRAM Type FCRAM

Organization (W × b)	Part Number	Initial Access Time Max. (ns)	Page Mode Access Time Max. (ns)	Burst Mode Frequency Max. (MHz)	Burst Clock Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)
						Operating (mA)	Standby (μA)	Power Down (μA)	
1M × 16	MB82D01181E-60L *1	60	N/A	N/A	N/A	20	100 *3	10	2.3 to 3.5
	MB82DS01181E-70L *2	70	N/A	N/A	N/A	20	100	10	1.7 to 1.95

*1: Shipping form: Chip, wafer, 48-pin FBGA package (SRAM compatible pinout)
*2: Shipping form: Chip, wafer
Package support for mass production is T.B.D.
*3: At $V_{DD} \leq 3.1V$

• 32M-bit Async. /Sync. SRAM Type FCRAM

*1, *2, *3

Organization (W × b)	Part Number	Initial Access Time Max. (ns) *4	Page Mode Access Time Max. (ns)	Burst Mode Frequency Max. (MHz)	Burst Clock Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)
						Operating (mA)	Standby (μA)	Power Down (μA)	
2M × 16	MB82DP02183E-65L	65	20	N/A	N/A	30	120	10	2.6 to 3.1
	MB82DBS02163E-70L	70	20	83	8 *5	30	120	10	1.7 to 1.95
	MB82DBS02154E-70L	70	N/A	104	7 *6	30	120	10	1.7 to 1.95

*1: Compliant with COSMORAM spec
*2: MB82DP02183E : with Page mode
MB82DBS02163E : with SDR Burst mode & Page mode
MB82DBS02154E : with SDR Burst mode & Multiplexed Address and Data Bus
*3: Shipping form: Chip, wafer, 71-pin FBGA package
*4: At asynchronous operation
*5: At RL = 5, 6
*6: At RL = 7

• 64M-bit Async. /Sync. SRAM Type FCRAM

*1, *2, *3

Organization (W × b)	Part Number	Initial Access Time Max. (ns) *4	Page Mode Access Time Max. (ns)	Burst Mode Frequency Max. (MHz)	Burst Clock Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)
						Operating (mA)	Standby (μA)	Power Down (μA)	
4M × 16	MB82DP04184E-65L	65	20	N/A	N/A	40	200	10	2.6 to 3.1
	MB82DBS04164E-70L	70	20	104	7 *5	40	200	10	1.7 to 1.95
	MB82DBS04154E-70L	70	N/A	104	7 *5	40	200	10	1.7 to 1.95

*1: Compliant with COSMORAM spec
*2: MB82DP04184E : with Page mode
MB82DBS04164E : with SDR Burst mode & Page mode
MB82DBS04154E : with SDR Burst mode & Multiplexed Address and Data Bus
*3: Shipping form: Chip, wafer
Package (71-pin FBGA) support for mass production is T.B.D.
*4: At asynchronous operation
*5: At RL = 6, 7

FCRAM™ (Fast Cycle RAM) (2)

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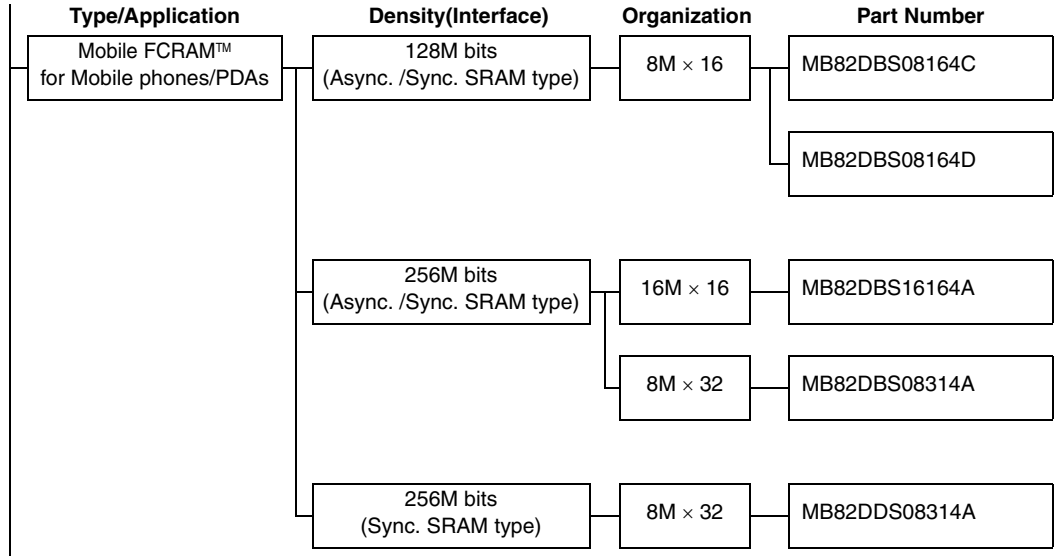

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FCRAM is a trademark of Fujitsu Microelectronics Limited.

FCRAM™ (Fast Cycle RAM) (2)

• 128M-bit Async. /Sync. SRAM Type FCRAM

*1, *2

Organization (W × b)	Part Number	Initial Access Time Max. (ns) *3	Page Mode Access Time Max. (ns)	Burst Mode Frequency Max. (MHz)	Burst Clock Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)
						Operating (mA)	Standby (μA)	Power Down (μA)	
8M × 16	MB82DBS08164C-70L	70	N/A	104	6 *4	40	300	10	1.7 to 1.95
	○ MB82DBS08164D-70L	70	N/A	104	6 *4	35 *5	200	10	1.7 to 1.95

○ : New Product

*1: Compliant with COSMORAM spec, with SDR Burst mode
*2: Shipping form: Chip, wafer
Package support for mass production is T.B.D.
*3: At asynchronous operation
*4: At RL = 6, 7
*5: $T_A \leqq +40$ °C

• 256M-bit Async. /Sync. SRAM Type FCRAM

*1, *2

Organization (W × b)	Part Number	Initial Access Time Max. (ns) *3	Page Mode Access Time Max. (ns)	Burst Mode Frequency Max. (MHz)	Burst Clock Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)
						Operating (mA)	Standby (μA)	Power Down (μA)	
16M × 16	MB82DBS16164A-80L	80	N/A	100	7 *4	40	250 *5	10	1.7 to 1.95
8M × 32	MB82DBS08314A-80L	80	N/A	100	7 *4	40	250 *5	10	1.7 to 1.95

*1: Compliant with COSMORAM spec, with SDR Burst mode
*2: Shipping form: Chip, wafer
Package(115-pin FBGA) support for mass production is T.B.D.
*3: At asynchronous operation
*4: At RL = 7, 8
*5: $T_A \leqq +40$ °C

• 256M-bit Sync. SRAM Type FCRAM

*1, *2

Organization (W × b)	Part Number	Initial Access Time Max. (ns) *3	Page Mode Access Time Max. (ns)	Burst Mode Frequency Max. (MHz)	Burst Clock Access Time Max. (ns)	Supply Current Max.			Supply Voltage (V)
						Operating (mA)	Standby (μA)	Power Down (μA)	
8M × 32	MB82DDS08314A-75L	45	N/A	135	6 *4	40	250 *5	10	1.75 to 1.95

*1: Compliant with COSMORAM spec, with DDR Burst mode & Multiplexed Address and Data Bus
*2: Shipping form: Chip, wafer
Package(115-pin FBGA) support for mass production is T.B.D.
*3: At Burst mode
*4: Data access time from CLK, $\overline{CLK}$
*5: $T_A \leqq +40$ °C

FCRAM™ (Fast Cycle RAM) (3)

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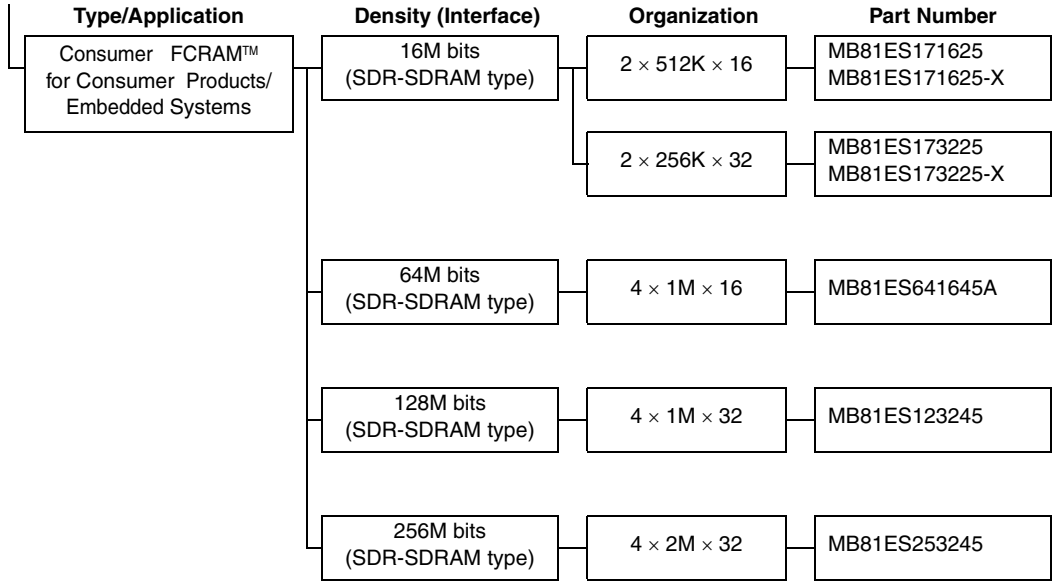


FCRAM is a trademark of Fujitsu Microelectronics Limited.

Consumer FCRAM™ (Fast Cycle RAM)

• 16M-bit SDR-SDRAM Type FCRAM

*1, *2

Organization (Bank × W × b)	Part Number	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *4	Supply Current Max. *5		Supply Voltage (V)
					Operating (mA)	Standby (mA)	
2 × 512K × 16	MB81ES171625-12	85	11.7	10.2	30	1	1.65 to 1.95
	MB81ES171625-15	66.7	15	12	30	1	1.65 to 1.95
	MB81ES171625-15-X *3	66.7	15	12	30	1	1.65 to 1.95
2 × 256K × 32	MB81ES173225-12	85	11.7	10.2	30	1	1.65 to 1.95
	MB81ES173225-15	66.7	15	12	30	1	1.65 to 1.95
	MB81ES173225-15-X *3	66.7	15	12	30	1	1.65 to 1.95

*1: Single Data Rate SDRAM Interface
*2: Shipping form: Chip, wafer
*3: Extended operating temperature
*4: Access Time = t_{AC}
*5: Operating current is I_{DD1} (1 bank active) and Standby current is I_{DD2P} (Power down mode)

• 64M-bit SDR-SDRAM Type FCRAM

*1, *2

Organization (Bank × W × b)	Part Number	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *3	Supply Current Max.		Supply Voltage (V)
					Operating (mA)	Standby (mA)	
4 × 1M × 16	○ MB81ES641645A-07	135	7.4	6.5	T.B.D.	T.B.D.	1.7 to 1.95

○ : New Product

*1: Single Data Rate SDRAM Interface
*2: Shipping form: Chip, wafer, 54-pin FBGA package
*3: Access Time = t_{AC}

• 128M-bit SDR-SDRAM Type FCRAM

*1, *2

Organization (Bank × W × b)	Part Number	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *3	Supply Current Max. *4		Supply Voltage (V)
					Operating (mA)	Standby (mA)	
4 × 1M × 32	MB81ES123245-10	108	9.2	7	*5	0.5	1.7 to 1.9

*1: Single Data Rate SDRAM Interface
*2: Shipping form: Chip, wafer
*3: Access Time = t_{AC}
*4: Operating current is I_{DD1} (1 bank active) and Standby current is I_{DD2P} (Power down mode)
*5: 60 (256 page length) , 45 (128 page Length) , 35 (64 page length)

• 256M-bit SDR-SDRAM Type FCRAM

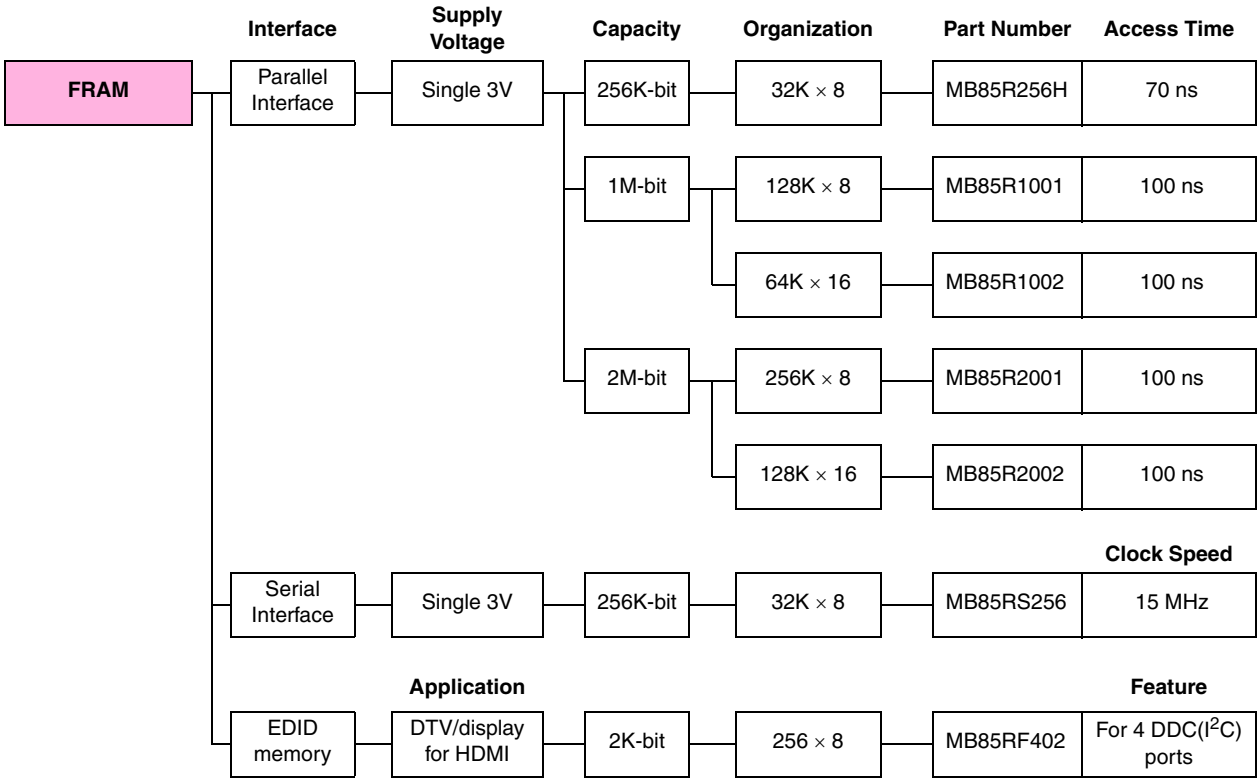
*1, *2

Organization (Bank × W × b)	Part Number	Clock Frequency Max. (MHz)	Clock Period Min. (ns)	Access Time Max. (ns) *3	Supply Current Max.		Supply Voltage (V)
					Operating (mA)	Standby (mA)	
4 × 2M × 32	◎ MB81ES253245	166	6	6	T.B.D.	T.B.D.	1.7 to 1.95

◎: Under development

*1: Single Data Rate SDRAM Interface
*2: Shipping form: Chip, wafer
*3: Access Time = t_{AC}

FRAM (Ferroelectric RAM)



FRAM

Interface	Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	Clock Speed Max. (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages		
						Operating (mA)	Standby (μA)			SOP	TSOP	FBGA
Parallel	32K × 8	MB85R256H	70	150	–	5	5	2.7 to 3.6	-40 to +85	28P	28P	-
Parallel	128K × 8	MB85R1001	100	150	–	10	10	3.0 to 3.6	-20 to +85	-	48P	-
Parallel	64K × 16	MB85R1002	100	150	–	10	10	3.0 to 3.6	-20 to +85	-	48P	48P
Parallel	256K × 8	MB85R2001	100	150	–	10	10	3.0 to 3.6	-20 to +85	-	48P	-
Parallel	128K × 16	MB85R2002	100	150	–	10	10	3.0 to 3.6	-20 to +85	-	48P	-
Serial	32K × 8	MB85RS256	–	–	15	5	3	3.0 to 3.6	-20 to +85	8P	-	-

Pakage : P – Plastic

EDID memory

Part Number	Memory	Organization (W × b)	Interface	Supply Voltage (V)	Packages
					TSSOP
○ MB85RF402	FRAM	256 × 8	For 4 DDC(I^2C) ports	3.8 to 5.5	16P

○ : New released.

Pakage : P – Plastic

Flash Memory (Single 1.8V)

SPANSION™ Products

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory	Single 1.8V	8 M bit	1 M × 8 512K × 16	S29AS008J	PD	50 to 70 ns	-
		16 M bit	2 M × 8 1 M × 16	S29AS016J	PD	50 to 70 ns	-

SPANSION™ Products

Flash memory (Single 1.8V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
				Read (mA)	Standby Mode (μA)			TSOP	FBGA
1 M × 8 512 K × 16	◎ S29AS008J50	50	50	16 (f = 5 MHz)	5	1.65 to 1.95	-40 to +85	48P	48P
	◎ S29AS008J70	70	70						
2 M × 8 1 M × 16	◎ S29AS016J50	50	50	16 (f = 5 MHz)	5	1.65 to 1.95	-40 to +85	48P	48P
	◎ S29AS016J70	70	70						

◎: Under Developing Package: P-Plastic

Flash Memory (Single 3V)

SPANSION™ Products

Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory — Single 3V	4M-bit	512K × 8 256K × 16	S29AL004D	PD	70 to 90 ns	*1
	8M-bit	1M × 8 512K × 16	S29AL008D	PD	70 to 90 ns	*2
			S29AL008J	PD	45 to 55 ns	*2
	16M-bit	2M × 8 1M × 16	S29AL016D	PD	70 to 90 ns	*3
			S29AL016J	PD	45 to 55 ns	*3
	32M-bit	4M × 8 2M × 16	S29AL032D	PD	70 to 90 ns	*4
			S29JL032H	PD SRW	70 to 90 ns	*5
			S29PL032J	PD PM SRW	55 to 70 ns	*6
	64M-bit	8M × 8 4M × 16	S29JL064H	PD SRW	70 to 90 ns	*6
			S29PL064J	PD PM SRW	55 to 70 ns	*6
	128M-bit	8M × 16	S29PL127J	PD PM SRW	55 to 70 ns	*10

Variation
PD: Automatic sleep mode
PM: Page mode
SRW: Simultaneous Read / Write operation (Read-while-program or Read-while-Erase)

MirrorBit is a trademark of Spansion Inc.

*1 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors) + (32Kbytes × 1sector) + (64Kbytes × 7sectors)
*2 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors) + (32Kbytes × 1sector) + (64Kbytes × 15sectors)
*3 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors + (32Kbytes × 1sector) + (64Kbytes × 31sectors)
*4 : (16Kbytes × 1sectors) + (8Kbytes × 2sectors + (32Kbytes × 1sector) + (64Kbytes × 61sectors)
*5 : (8Kbytes × 8sectors) + (64Kbytes × 63sectors)
*6 : (8Kbytes × 16sectors) + (64Kbytes × 126sectors)
*7 : (8Kbytes × 8sectors) + (64Kbytes × 127sectors)
*8 : (64Kbytes × 128sectors)
*9 : (8Kbytes × 16sectors) + (64Kbytes × 62sectors)
*10 : (8Kbytes × 16sectors) + (64Kbytes × 254sectors)

SPANSION™ Products

Flash memory (Single 3V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages		
				Read (mA)	Standby Mode (μA)			TSOP	FBGA	SOP
512K × 8 256K × 16	S29AL004D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	44P
	S29AL004D90	90	90							
1M × 8 512K × 16	S29AL008D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	44P
	S29AL008D90	90	90							
	◎ S29AL008J45	45	45	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	44P
	◎ S29AL008J55	55	55							
2M × 8 1M × 16	S29AL016D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	–
	S29AL016D90	90	90							
	◎ S29AL016J45	45	45	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	44P
	◎ S29AL016J55	55	55							
4M × 8 2M × 16	S29AL032D70 *	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	48P	48P
	S29AL032D90	90	90							
	S29JL032H70	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	–	–
	S29JL032H90	90	90							
	S29PL032J55	55	55	30 (f = 5 MHz)	5	2.7 to 3.6	-45 to +85	–	48P 56P	–
	S29PL032J60	60	60							
	S29PL032J65	65	65							
	S29PL032J70	70	70							
8M × 8 4M × 16	S29JL064H70	70	70	16 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P	–	–
	S29JL064H90	90	90							
	S29PL064J55	55	55	30 (f = 5 MHz)	5	2.7 to 3.6	-45 to +85	–	48P 56P	–
	S29PL064J60	60	60							
	S29PL064J65	65	65							
	S29PL064J70	70	70							
8M × 16	S29PL127J55	55	55	30 (f = 5 MHz)	5	2.7 to 3.6	-45 to +85	56P	50P	–
	S29PL127J60	60	60							
	S29PL127J65	65	65			2.7 to 3.6 1.65 to 1.95				
	S29PL127J70	70	70							

◎: Under Developing

* : at C_L = 30pF

Package: P-Plastic

Flash Memory (MirrorBit™) (Single 3 V)

SPANSION™ Products

Flash Memory MirrorBit™	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
	Single 3V	32M-bit	4M × 8 2M × 16	S29GL032A	PD PM WB	90 to 110 ns	*1
				S29GL032N	PD PM WB	90 ns	*1
		64M-bit	8M × 8 4M × 16	S29GL064A	PD PM WB	90 to 110 ns	*2
				S29GL064N	PD PM WB	90 ns	*2
		128M-bit	16M × 8 8M × 16	S29GL128N	PD PM WB	90 to 110 ns	*3
				S29GL128P	PD PM WB	90 to 110 ns	*3
		256M-bit	32M × 8 16M × 16	S29GL256N	PD PM WB	90 to 110 ns	*4
				S29GL256P	PD PM WB	90 to 110 ns	*4
		512M-bit	64M × 8 32M × 16	S29GL512N	PD PM WB	100 to 110 ns	*5
				S29GL512P	PD PM WB	100 to 110 ns	*5
		1G-bit	128M × 8 64M × 16	S29GL01GP	PD PM WB	110 to 130 ns	*6

Variation
PD : Automatic sleep mode
PM: Page mode
WB: Write buffer

MirrorBit is a trademark of Spansion Inc.

*1: Uniform sector model : 32Kword (64Kbytes) × 64sectors
Boot sector model : 32Kword (64Kbytes) × 63sectors + 4Kword (8Kbytes) × 8sectors
*2: Uniform sector model : 32Kword (64Kbytes) × 128sectors
Boot sector model : 32Kword (64Kbytes) × 127sectors + 4Kword (8Kbytes) × 8sectors
*3: Sector structure - 64Kword (128Kbytes) × 128sectors
*4: Sector structure - 64Kword (128Kbytes) × 256sectors
*5: Sector structure - 64Kword (128Kbytes) × 512sectors
*6: Sector structure - 64Kword (128Kbytes) × 1024sectors

SPANSION™ Products

Flash memory (MirrorBit) (Single 3V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Cycle Time Min. (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
				Read (mA)	Standby Mode (μA)			TSOP	FBGA
4M × 8 2M × 16	S29GL032A90	90 (25)	90	25 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	40P 48P 56P	48P 64P
	S29GL032A10	100 (30)	100						
	S29GL032A11	110 (30)	110						
	S29GL032N90	90 (25)	90	40 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P 56P	48P 56P
8M × 8 4M × 16	S29GL064A90	90 (25)	90	25 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	48P 56P	64P
	S29GL064A10	100 (30)	100						
	S29GL064A11	110 (30)	110						
	S29GL064N90	90 (25)	90	40 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	48P 56P	48P 56P
16M × 8 8M × 16	S29GL128N90	90 (25)	90	50 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	56P	64P
	S29GL128N10	100 (25)	100			2.7 to 3.6			
	S29GL128N11	110 (30)	110						
	S29GL128P90	90 (25)	90	50 (f = 5 MHz)	5	3.0 to 3.6	0 to +70 -40 to +85	56P	64P
	S29GL128P10	100 (25)	100			2.7 to 3.6	-40 to +85		
	S29GL128P11	110 (25)	110						
32M × 8 16M × 16	S29GL256N90	90 (25)	90	50 (f = 5 MHz)	5	3.0 to 3.6	-40 to +85	56P	64P
	S29GL256N10	100 (25)	100			2.7 to 3.6			
	S29GL256N11	110 (30)	110						
	S29GL256P90	90 (25)	90	50 (f = 5 MHz)	5	3.0 to 3.6	0 to +70 -40 to +85	56P	64P
	S29GL256P10	100 (25)	100			2.7 to 3.6	-40 to +85		
	S29GL256P11	110 (25)	110						
64M × 8 32M × 16	S29GL512N10	100 (25)	100	50 (f = 5 MHz)	5	2.7 to 3.6	-40 to +85	56P	64P
	S29GL512N11	110 (30)	110						
	S29GL512P10	100 (25)	100	50 (f = 5 MHz)	5	3.0 to 3.6	0 to +70 -40 to +85	56P	64P
	S29GL512P11	110 (25)	110			2.7 to 3.6	-40 to +85		
	S29GL512P12	120 (25)	120						
128M × 8 64M × 16	S29GL01GP11	110 (25)	110	50 (f = 5 MHz)	5	3.0 to 3.6	0 to +70 -40 to +85	56P	64P
	S29GL01GP12	120 (25)	120			2.7 to 3.6	-40 to +85		
	S29GL01GP13	130 (25)	130						

C_L = 30pF

Package: P-Plastic

Flash Memory (MirrorBit™) (Single 1.8V)

SPANSION™ Products

Flash Memory MirrorBit™	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
	Single 1.8V	128 M-bit	8 M × 16	S29WS128N	PD BM SRW HM	9.0 (80 MHz) to 13.5 (54 MHz) ns	*1
				S29WS128P	PD BM SRW HM	7.6 (80 MHz) to 13.5 (54 MHz) ns	*1
		256 M-bit	16 M × 16	S29SW256N	PD BM SRW HM	9.0 (80 MHz) to 13.5 (54 MHz) ns	*2
				S29WS256P	PD BM SRW HM	7.6 (80 MHz) to 13.5 (54 MHz) ns	*2
		512 M-bit	32 M × 16	S29WS512P	PD BM SRW HM	7.6 (80 MHz) to 13.5 (54 MHz) ns	*3

Variation
PD: Automatic sleep mode
BM: Burst mode
SRW: Simultaneous Raad/Write operation
(Read-while-program or Read-while-Erase)
HM: Hand Shake Mode

*1 : 16 Kword × 8sectors + 64 Kword × 126sectors
*2 : 16 Kword × 8sectors + 64 Kword × 254sectors
*3 : 16 Kword × 8sectors + 64 Kword × 510sectors

MirrorBit is a trademark of Spansion Inc.

SPANSION™ Products

Flash memory (MirrorBit) (Single 1.8V)

Organization (W × b)	Part Number	Access Time Max. (ns)	Burst Speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages
				Read (mA)	Standby Mode (μA)			FBGA
8 M × 16	S29WS128N0LBxW	80 *1 80/13.5 *2	54	36 *3	70	1.70 to 1.95	-25 to +85	84P
	S29WS128N0PBxW	80 *1 80/11.2 *2	66	42 *3				
	S29WS128N0SBxW	80 *1 80/9.0 *2	80	48 *3				
	S29WS128P0LBxW	80 *1 80/13.5 *2	54	39 *3				
	S29WS128P0PBxW	80 *1 80/11.2 *2	66	43 *3				
	S29WS128P0SBxW	80 *1 80/9.0 *2	80	48 *3				
	S29WS128PABBxW	80 *1 80/7.6 *2	108	54 *3				
16 M × 16	S29WS256N0LBxW	80 *1 80/13.5 *2	54	36 *3	70	1.70 to 1.95	-25 to +85	84P
	S29WS256N0PBxW	80 *1 80/11.2 *2	66	42 *3				
	S29WS256N0SBxW	80 *1 80/9.0 *2	80	48 *3				
	S29WS256P0LBxW	80 *1 80/13.5 *2	54	39 *3				
	S29WS256P0PBxW	80 *1 80/11.2 *2	66	43 *3				
	S29WS256P0SBxW	80 *1 80/9.0 *2	80	48 *3				
	S29WS256PABBxW	80 *1 80/7.6 *2	108	54 *3				
32 M × 16	S29WS512P0LBxW	80 *1 80/13.5 *2	54	36 *3	70	1.70 to 1.95	-25 to +85	84P
	S29WS512P0PBxW	80 *1 80/11.2 *2	66	43 *3				
	S29WS512P0SBxW	80 *1 80/9.0 *2	80	48 *3				
	S29WS512PABBxW	80 *1 80/7.6 *2	108	54 *3				

C_L = 30pF

Package: P-Plastic

*1: Asynchronous access time

*2: Synchronous delay time/burst access time

*3: At burst read Continuous mode (Max.)

Serial Peripheral Interface (MirrorBit™) (Single 3V)

SPANSION™ Products

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory MirrorBit™	Single 3V	4 M-bit	4 M × 1	S25FL040A	SI	50 MHz	*1
		8 M-bit	8 M × 1	S25FL008A	SI	50 MHz	*2
		16 M-bit	16 M × 1	S25FL016A	SI	50 MHz	*3
		32 M-bit	32 M × 1	S25FL032A	SI	50 MHz	*4
		64M-bit	64 M × 1	S25FL064A	SI	50 MHz	*5
		128M-bit	128 M × 1	S25FL128P	SI	104 MHz	*6

Variation
SI: Serial interface

*1 : Sector structure - 512 K bits × 8 sectors or 128 K bits × 2 sectors + 32 K bits × 2 sectors + 16 K bits × 2 sectors + 512 K bits × 7 sectors
*2 : Sector structure - 512 K bits × 16 sectors
*3 : Sector structure - 512 K bits × 32 sectors
*4 : Sector structure - 512 K bits × 64 sectors
*5 : Sector structure - 512 K bits × 128 sectors
*6 : Sector structure - 512 K bits × 256 sectors

MirrorBit is a trademark of Spansion Inc.

SPANSION™ Products

Flash memory (MirrorBit) (Single 3V)

Organization (W × b)	Part Number	Clock speed (MHz)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
			Read (mA)	Standby Mode (μA)			SOIC	SON
4 M × 1	S25FL040A	50	13 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	SOIC8	USON8
8 M × 1	S25FL008A	50	13 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	SOIC8	USON8
16 M × 1	S25FL016A	50	19 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	SOIC8 SOIC16	WSON8 –
32 M × 1	S25FL032A	50	19 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	SOIC16	–
64 M × 1	S25FL064A	50	13 (f = 50MHz)	50	2.7 to 3.6	-40 to +85	SOIC16	–
128 M × 1	S25FL128P	104	22 (f = 104MHz)	200	2.7 to 3.6	-40 to +85	SOIC16	WSON

C_L = 30pF
Package: P-Plastic

Flash Memory (MirrorBit™ ORNAND™) (Single 1.8V)

SPANSION™ Products

	Supply Voltage	Capacity	Organization	Part Number	Variation	Access Time	Remarks
Flash Memory (MirrorBit™ ORNAND™)	Single 1.8V	512 M-bit	32 M × 16 64 M × 8	S30MS512P	ND	8 µs/25 ns	*
				S30MS512R	ND	8 µs/25 ns	*
		1 G-bit	64 M × 16 128 M × 8	S30MS01GP	ND	8 µs/25 ns	*
				S30MS01GR	ND	8 µs/25 ns	*
		2 G-bit	128 M × 16 256 M × 8	S30MS02GR	ND	8 µs/25 ns	*

Variation
ND: NAND interface

* : Block size 128 K + 4 Kbyte

MirrorBit is a trademark of Spansion Inc.

ORNAND is a trademark of Spansion Inc.

SPANSION™ Products

Flash memory (MirrorBit ORNAND) (Single 1.8V)

Organization (W × b)	Part Number	Page Access (µs)	Serial Read (ns)	V_{CC} Current		Supply Voltage (V)	Operating Temperature Range T_A (°C)	Packages	
				Read (mA)	Standby Mode (µA)			TSOP	BGA
64 M × 8	S30MS512P25BFW00	8	25	45	60	1.70 to 1.95	-25 to +85	48P	137P
	S30MS512P25TFW00	8	25						
	○ S30MS512R25TFW00	8	30	50					-
	○ S30MS01GR25TFW01	8	30						
32 M × 16	S30MS512P25BFW01	8	25	45	60	1.70 to 1.95	-25 to +85	48P	137P
	S30MS512P25TFW01	8	25						
	○ S30MS512R25TFW01	8	30	50					-
128 M × 8	S30MS01GP25BFW00	8	25	45	60	1.70 to 1.95	-25 to +85	48P	137P
	S30MS01GP25TFW00	8	25						
	○ S30MS01GR25TFW00	8	30	50					-
	○ S30MS02GR25TFW01	8	30						
64 M × 16	S30MS01GP25BFW01	8	25	45	60	1.70 to 1.95	-25 to +85	48P	137P
	S30MS01GP25TFW01	8	25						
256 M × 8	○ S30MS02GR25TFW00	8	30	50	60	1.70 to 1.95	-25 to +85	48P	-

○ : New Product

Package: P-Plastic

C_L = 30pF

Products Scheduled to be out of Production

The productions listed below are scheduled to go out of production.
If you are considering the use in the new applications, select the other series of products

FCRAM

Part number	Description
MB82DP02183C-65L	32 Mbit Async. SRAM Type FCRAM
MB82DBS02163C-70L	32 Mbit Async./Sync. SRAM Type FCRAM
MB82DP04183C-65L	64 Mbit Async. SRAM Type FCRAM
MB82DP04183D-65L	
MB82DBS04163C-70L	64 Mbit Async./Sync. SRAM Type FCRAM
MB82DBS04163D-70L	
MB82DBS04314C-70L	128 Mbit Async./Sync. SRAM Type FCRAM

ASIC Product Line-up

ASIC Products

ASIC Products					Page No.
	Standard cell	CMOS	CS201 series	with on-chip RAM, ROM, ADC/DAC	74
			CS101 series	More than 91,000,000 (on-chip) gates with on-chip RAM, ROM, ADC/DAC	75
			CS91 series	More than 48,000,000 (on-chip) gates with on-chip RAM, ROM, Multipliers, ADC/DAC	76
			CS86 series	More than 40,000,000 (on-chip) gates with on-chip RAM, ROM, FIFO, Delay Line, ADC/DAC	77
			CS81 series	More than 40,000,000 (on-chip) gates, 11 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	78
			CS66 series	More than 1,700,000 (on-chip) gates, 98 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	79
	Macro-embedded type cell arrays	CMOS	CE81 series	Maximum of 34,000,000 (on chip) gates, 12 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	81
			CE77 series	Maximum of 10,000,000 (on chip) gates, 33 ps/gate with on-chip RAM, ROM, FIFO, Delay Line	82
			CE71 series	Maximum of 8,096,000 (on chip) gates, 29 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC	84
			CE66 series	Maximum of 1,138,000 (on-chip) gates, 98 ps/gate with on-chip RAM, ROM, Multipliers, ADC/DAC.	86
			CE61 series	Maximum of 2,025,000 (on chip) gates, 85 ps/gate with on-chip RAM/ROM, Multipliers, ADC/DAC	88
	Gate arrays	Sea-of-Gate CMOS	CG61 series	Maximum of 1,568,000 (on chip) gates, 85 ps/gate with on-chip RAM, Analog PLL embedment is possible in some frames	90
			CG47 series	Maximum of 55,000 (on chip) gates, 300 ps/gate with on-chip RAM, FIFO	91
			CG46 series	Maximum of 198,000 (on chip) gates, 300 ps/gate with on-chip RAM, FIFO	92

CS201 Series

Features

Technology : 65 nm Si-gate CMOS
6- to 12-metal layers. Low-k (low permittivity) inter-layer insulation film material is used for all layers.
Consolidation of all 3 kinds of set of cell (energy-saving version to high-velocity version) is possible.
Supply voltage : +1.2 V ± 0.1 V , +1.0 V ± 0.1 V
Junction temperature range : -40 °C to +125 °C
Reduced chip sized realized by I/O with pad.
Supports a wide range of cell sets (from low power versions to high speed versions)
IP macros : CPU (ARM11, ARM9, ARM7TDMI), DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM and others)
It supports energy-saving mode, multi mode SRAM.
It supports energy-saving technology "CoolAdjust"*
Supports large capacity memory (1T-SRAM-Q)
High-speed interface macro (up to 10 Gbps)
Special interfaces (LVDS, SSTL and others)
Supports use of industry standard libraries (. LIB)
Uses industry standard tools and supports the optimum tools for the application.
High reliability design estimation in the early stage of physical design realized by physical prototyping tool.
Layout synthesis with optimized timing realized by physical synthesis tools.
Hierarchical design environment for supporting large-scale circuits.
High accuracy design environment considering dynamic drop in power supply voltages, signal noise, delay penalty, and crosstalk.
I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.
Supports static timing sign-off
Improved timing settling by introducing Statistical Timing Analysis (SSTA).
Steady product supply and countermeasure for diffusion by introduction of DFM
Supports memory (RAM/ROM) BIST
Supports boundary SCAN
Supports LOGIC BIST
Supports transition delay test
Optimum of package lineup : TEBGA, FBGA, PBGA, FC-BGA

*: "CoolAdjust" is a generic name of Fujitsu Microelectronics's energy-saving technology

Note: Some items are in preparation.

CS101 Series

Features

Optimum gate count : Maximum of 91,000,000 gates
Technology : 90 nm Si-gate CMOS
6- to 10-metal layers. Low-k (low permittivity) inter-layer insulation film material is used for all layers.
3 types of transistors (low leak, standard, high speed) can be mixed on a chip.
The design rules comply with industry standard processes.
Supply voltage : +1.2 V ± 0.1 V, +1.0 V ± 0.1 V
Junction temperature range : -40 °C to +125 °C (normal)
Gate delay time : tpd = 12 ps (1.2 V, Inverter, F/O = 1)
Gate power consumption : Pd = 2.7 nW/MHz/BC (1.2 V, Inverter, F/O = 1)
Reduced chip sized realized by I/O with pad.
Supports a wide range of cell sets (from low power versions to high speed versions)
Compliance with industry standard design rules enables non-Fujitsu commercial macros to be easily incorporated.
IP macros : CPU (ARM9, ARM7TDMI) , DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM and others)
High-speed interface macro (up to 10 Gbps)
Special interfaces (LVDS, SSTL_2 and others)
Supports use of industry standard libraries (. LIB)
Uses industry standard tools and supports the optimum tools for the application.
High reliability design estimation in the early stage of physical design realized by physical prototyping tool.
Layout synthesis with optimized timing realized by physical synthesis tools.
Hierarchical design environment for supporting large-scale circuits.
High accuracy design environment considering drop in power supply voltages, signal noise, delay penalty, and crosstalk.
I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.
Supports static timing sign-off
Supports memory (RAM/ROM) BIST
Supports boundary SCAN
Supports LOGIC BIST
Supports transition delay test

Optimum of package lineup : TEBGA, FBGA, PBGA, FC-BGA

Note: Some items are in preparation.

CS91 Series

Features

Optimum gate count : Maximum of 48,000,000 gates
Technology : 0.11 μm Si-gate CMOS, 5- to 8-layer wiring (Copper is used as wire material) ,
Low-k Inter-layer material
(Inter-layer material that has low permittivity)
Supports 8 types of cell sets that differ in speed, integration, and power consumption.
These cell sets can be mixed on a chip.
Supply voltage : +1.2 V ± 0.1 V (normal)
Junction temperature range : -40 to +125 °C
Gate delay time : tpd = 16 ps (1.2 V, Inverter, F/O = 1)
Gate power consumption : Pd = 6.6 nW/MHz (1.2 V, Inverter, F/O = 1)
High-speed interface macro (up to 10 Gbps)
Special interfaces: P-CML, LVDS, PCI, USB, SSTL, HSTL, T-LVTTL, and others
Buffer cells for crystal oscillation circuits.
IP macros : CPU (ARM9, ARM7TDMI) , DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM/multiplier and others)
Uses industry standard tools and supports the optimum tools for the application.
Short-term development using a physical prototyping tool.
Hierarchical design environment for supporting large-scale circuits.
Supports Signal Integrity, EMI noise reduction
Supports High resolution RC extraction base delay calculation environment
Supports optimization environment of power supply wire
Supports static timing sign-off
Supports memory (RAM/ROM) BIST
Supports boundary SCAN
Supports LOGIC BIST
Supports transition delay test
A variety of package options : FC-BGA (Max. 2116 pin), EBGA, HQFP, FBGA and others

Note: Some items are in preparation.

CS86 Series

Features

Optimum gate count	: Maximum of 40,000,000 gates		
Technology	: 0.18 μm Si-gate CMOS, 4- to 6-layer wiring		
	Supports three types of internal cell sets (ultra high-speed, standard, low-leak)		
	Capable of integrating a mixture of standard transistor cell and ultra high-speed process/cell, and mixture of standard transistor cell and low leak process/cell on a single chip		
Supply voltage	: +1.8 V ± 0.15V (normal) to +1.1V ± 0.1V		
Gate delay time	: tpd = 88 ps	(standard	: 1.8 V, 2NAND, F/O = 2, standard load)
	tpd = 70 ps	(ultra high-speed	: 1.8 V, 2NAND, F/O = 2, standard load)
	tpd = 136 ps	(low-leak	: 1.8 V, 2NAND, F/O = 2, standard load)
Leakage Current	: 0.023 nW	(standard	: 1.8 V, 2NAND, F/O = 0, no load)
	3.922 nW	(ultra high-speed	: 1.8 V, 2NAND, F/O = 0, no load)
	0.0067 nW	(low-leak	: 1.8 V, 2NAND, F/O = 0, no load)
Gate power consumption	: 40.1 nW/MHz	(standard	: 1.8 V, 2NAND, F/O = 1, 4Grid)
	42.7 nW/MHz	(ultra high-speed	: 1.8 V, 2NAND, F/O = 1, 4Grid)
	38.3 nW/MHz	(low-leak	: 1.8 V, 2NAND, F/O = 1, 4Grid)
Junction temperature range	: -40 to +125 °C		

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.

Special interfaces	: SSTL2, PCI, P-CML, T-LVTTL, USB2.0, IEEE1394, and others
IP macros	: CPU (FR-V, ARM9,and others), DSP, PCI, IEEE1394, USB2.0, IrDA, PLL, ADC, DAC, and others

Compiled cells (RAM/ROM/FIFO/Delay line, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a physical synthesis tool
Low-power dissipation using a low power synthesis tool
Short-term development using a timing driven layout tool
Hierarchical design environment for supporting large-scale circuits
Supports signal Integrity
Supports memory (RAM, ROM) SCAN
Supports memory (RAM) BIST
Supports boundary SCAN
Supports path delay test
Supports transition delay test
A variety of package options (QFP, TQFP, LQFP, HQFP, PBGA, FBGA, FLGA, EBGA)

Note: Some items are in preparation.

Packages

The table below lists the available package types.

Type	Pin Count	Material
QFP	176, 208, 240	Plastics
TQFP	100, 120	Plastics
LQFP	144, 176, 208, 256	Plastics
HQFP	208, 240, 256, 304	Plastics
PBGA	256, 352, 420	Plastics
FBGA	112, 144, 168, 176, 192, 224, 272, 288, 240, 304, 368	Plastics
FLGA	144, 176, 208, 224, 288	Plastics
EBGA	660	Plastics

Note: This list contains packages under planning. Contact Fujitsu Microelectronics for the availability.

CS81 Series

Features
Optimum gate count : Maximum of 40,000,000 gates
Technology : 0.18 μm Si-gate CMOS, 3- to 6-layer wiring
Capable of integrating a mixture of high-speed processes and cells on a single chip
Supply voltage : +1.8 V ± 0.15V (normal) to +1.1V ± 0.1V
Gate delay time : tpd = 11 ps (1.8 V, Inverter, F/O = 1)
Gate power consumption : 5nW/MHz/BC (1.1V, 2NAND, F/O = 1)
Junction temperature range : -40 to +125 °C
High-speed interface macro (up to 3.125 Gbps)
Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces: P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, and others
IP macros: CPU, DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM/multiplier, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a timing driven layout tool
Supports static timing sign-off
Dramatically reducing the time for generating test vectors for timing verification and the simulation time
Hierarchical design environment for supporting large-scale circuits
Simulation (before layout) considering the input through rate and high resolution RC extraction base delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supports signal Integrity, EMI noise reduction
Supports memory (RAM, ROM) SCAN
Supports memory (RAM) BIST
Supports boundary SCAN
Supports At-Speed test on internal circuits
Supports path delay test
Supports transition delay test
A variety of package options (TQFP, HQFP, EBGA, FBGA, TAB-BGA, FC-BGA, LQFP)

Note: Some items are in preparation.

Packages

The table below lists the available package types.

Type	Pin Count	Material
TAB-BGA	304, 352, 480 560, 660, 720	Plastics
EBGA	576, 660, 672	Plastics
HQFP	208, 240, 256, 304	Plastics
TQFP	100, 120	Plastics
LQFP	144, 176, 208	Plastics
FBGA	288	Plastics
FC-BGA	1089, 1225, 1369, 1681, 1849, 2116	Plastics, Ceramic

Note: This list contains packages under planning. Contact Fujitsu Microelectronics for the availability.

CS66 Series

Features

Optimum gate count	: Maximum of 1,700,000 gates
Technology	: 0.35 μm Si-gate, 3- to 4-layer metal wiring
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V +5.0 V ± 10% (only for external interface; when internal requirements is 3.3 V) +3.3 V ± 10% (only for external interface; when internal requirements is 3.3 to 2.0 V)
Gate delay time	: t_{pd} = 91 ps (high-speed type, F/O = 2, standard load)
Gate power consumption	: 0.29 μW/MHz (F/O = 2, standard load)
Junction temperature range	: -40 to +125°C
High-load driving capability	: I_{OL} = 2 mA/4mA/8mA/12mA/24mA mixable.

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (50 kΩ typical)
Buffer cells for crystal oscillation circuits.
Configurable internal bus circuits
Highly integrated RAM/ROM/multipliers mountable; arbitrary words/bits configurable.
Clock skew layout design method (Cadence "CT-Gen") based on the floor plan information minimizes post-layout circuit modification, reducing turnaround time for development.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Special interface (T-LVTTL and SDRAM-I/F, and others)
Analog PLL
Analog circuits (ADC, DAC, OPAMP and others)
Macros for system ASICs (CPU core, CPU peripheral, operation macro, and others)
Supports DFF scan test with MUX
Supports memory (RAM/ROM) scan
Supports memory (RAM) BIST
Supports boundary SCAN

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.

CS66 (P-frame)

Package and pin count		0 2000K 4000K 6000K 8000K 10000K 12000K 14000K 16000K
TQFP	100	1579K
LQFP	100	1579K
	144	1579K
	176	1579K
	208	1305K
QFP	120	1579K
	144	1579K
	160	1579K
	176	1579K
	208	1579K
	240	1579K
	256	1579K
HQFP	208	1579K
	240	1579K
	256	1579K
	304	1579K
PBGA	256	1579K
	352	1579K
FBGA	112	639K
	144	639K
	168	835K
	176	1305K
	192	1579K
	224	1579K
	288	1579K

Note: This list contains packages under planning.

CS66 (S-frame)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K
TQFP	100	158K
LQFP	100	158K
	144	158K
	208	433K
QFP	120	158K
	144	158K
	160	228K
	176	228K
	208	358K
	240	545K
HQFP	208	358K
	240	545K
	256	545K
PBGA	256	545K
	352	807K
FBGA	112	192K
	144	228K
	168	433K
	176	228K
	192	289K
	224	433K
	288	807K

Note: This list contains packages under planning.

CE81 Series

Features

High Integration : Maximum of 34,000,000 BCs
Technology : 0.18 μm Si-gate CMOS, 4- to 5-layer wiring
Supply voltage : +1.8 V ± 0.15 V (normal) to +1.1 V ± 0.1 V
Gate delay time : tpd = 12 ps (1.8V, Inverter, F/O = 1)
Gate power consumption : 8nW/MHz/BC (1.1V, 2NAND, F/O = 1)
Junction temperature range : -40 to +125 °C
Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces: P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, and others
IP macros: CPU, DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others
Compiled cells (RAM/ROM/multipliers, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a timing driven layout tool
Supports static timing sign-off
Dramatically reducing the time for generating test vectors for timing verification and the simulation time.
Hierarchical design environment for supporting large-scale circuits
Supports optimization environment of power supply wire
Simulation (before layout) considering of the input through rate and high resolution RC extraction base delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supports Signal Integrity
Supports memory (RAM, ROM) SCAN
Supports memory (RAM) BIST
Supports boundary SCAN
Supports At-Speed test on internal circuits
Supports path delay test
Supports transition delay test
A variety of package options (TQFP, HQFP, EBGA, FBGA, TAB-BGA, LQFP)
Note: Some items are in preparation.

Number of gates used in package

The table below lists the available package types and the reference number of gates used.

Package and pin count		0 2000K 4000K 6000K 8000K 10000K 12000K 14000K 16000K
TAB-BGA	304	891K
	352	1254K
	480	1905K
	560	2689K
	660	3609K
	720	9129K
EBGA	576	5982K
	660	9805K
	672	7952K
HQFP	208	1098K
	240	2085K
	256	3764K
	304	15158K
	304	4712K
TQFP	100	514K
	120	514K
LQFP	144	722K
	176	722K
	208	1098K
FBGA	288	4712K

Note: This list contains packages under planning.

CE77 Series

Features

High integration	: Maximum of 10,000,000 BCs
Technology	: 0.25 μm Si-gate CMOS, 3- to 4-layer wiring
Supply voltage	: +2.5 V ± 0.2 V (normal) to +1.5 V ± 0.1 V
Junction temperature range	: -40 to +125°C
Gate delay time	: t_{pd} = 33 ps (2.5 V, Inverter, F/O = 1, No load)
Gate power consumption	: 0.02 μW/MHz (1.5 V, Inverter, F/O = 1, No load)
High-load driving capability	: I_{OL} = 2mA/4mA/8mA/12mA mixable.

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (25 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces (P-CML, LVDS, T-LVTTL, SSTL, PCI, USB, GTL+, and others)
IP macros (CPU, PCI, USB, IrDA, PLL, DAC, ADC, and others)
Compiled cells (RAM/ROM/FIFO/Delay Line, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Short-term development using a timing driven layout tool
Hierarchical design environment for supporting large-scale circuits
Supports static timing sign-off
Dramatically reducing the time for generating test vectors for timing verification and the simulation time.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supports memory (RAM, ROM) SCAN
Supports memory (RAM) BIST
Supports boundary SCAN
Supports path delay test
A variety of package options (SQFP, LQFP, HQFP, FBGA, PBGA)

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.
CE77 (V-Frame)

Package and pin count		0 1000k 2000k 3000k 4000k 5000k 6000k 7000k 8000k 9000k	Material
SQFP	176	274k	P
	208	803k	P
	240	965k	P
HQFP	208	1776k	P
	240	2276k	P
	256	1776k	P
	304	7128k	P
PBGA	256	618k	P

P: Plastic
Note: This list contains packages under planning.

CE77 (T-Frame)

Package and pin count		0 500K 1000K 1500K 2000K 2500K 3000K 3500K 4000K 4500K 5000K	Material
LQFP	144	976 K	P
	176	744 K	P
	208	1375 K	P
	256	1841 K	P
HQFP	208	1375 K	P
	240	1609 K	P
	256	2109 K	P
	304	4538 K	P
FBGA	144	461 K	P
	176	646 K	P
	224	1375 K	P
	288	2109 K	P
PBGA	256	1841 K	P
	352	2678 K	P
	420	3789 K	P

P: Plastic
Note: This list contains packages under planning.

CE71 Series

Features

High integration	: Maximum of 8,000,000 BCs
Technology	: 0.25 μm Si-gate CMOS, 3- to 4-layer metal wiring
Supply voltage	: +2.5 V ± 0.2 V (normal) to +1.5 V ± 0.1 V (5 V TTL interface is available if 5 V tolerant I/O is adopted. Some frames are under development.)
Gate delay time	: t_{pd} = 29 ps (2.5 V, Inverter, F/O = 1, No load)
Gate power consumption	: 0.060 μW/MHz (F/O = 1, No load)
Junction temperature range	: -40 to +125°C
High-load driving capability	: I_{OL} = 2 mA/4 mA/8 mA/12 mA mixable.

Output buffer cells with noise reduction circuits
Inputs with on-chip input pull-up/pull-down resistors (25 kΩ typical) and bidirectional buffer cells.
Buffer cells for crystal oscillation circuits.
Special interfaces (P-CML, LVDS, SDRAM-I/F, SSTL, and others)
IP macros (SPARClite, FR40, F²MC16LX, PCI, IEEE1394, USB, IrDA, PLL, ADC/DAC, and others)
Compiled cells (RAM/ROM/multipliers, and others)
Configurable internal bus circuits
Advanced for hardware/software co-design environment
Linking floor plan tools and logic synthesis tools allows automatic optimization of the circuits using the floor plan information. The Clock Driven Design Method (CDDM) clock tree synthesis tools using the floor plan information are also available. Using the floor plan information in the pre-layout stage would eliminate the problems of setup after lay-out or timing problems for hold, significantly reducing the time to market.
Supports the static timing sign off using the Synopsys CAD tool Prime Time. This contributes to the considerable reduction of time required for test vector creation for timing verification and the simulation time.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Supports memory (RAM, ROM) SCAN
Supports memory (RAM) BIST
Supports boundary SCAN
A variety of package options (SQFP, LQFP, HQFP, PBGA, EBGA, TAB-BGA, FBGA)

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.
CE71 (J-Frame)

Package and pin count		0 — 1000 K — 2000 K — 3000 K — 4000 K — 5000 K	Material
SQFP	176	203 K	P
	208	592 K	P
	240	714 K	P
HQFP	208	1313 K	P
	240	1681 K	P
	256	1313 K	P
	304	5345 K	P
PBGA	256	457 K	P
EBGA	352	991 K	P
	420	1313 K	P
	576	1986 K	P
	660	5345 K	P
	672	2673 K	P

P: Plastic
Note: This list contains packages under planning.

CE71 (L-Frame)

Package and pin count		0 — 1000 K — 2000 K — 3000 K — 4000 K — 5000 K	Material
TAB-BGA	304	310 K	P
	352	672 K	P
	480	672 K	P
	560	2279 K	P
	660	1284 K	P
	720	3278 K	P

Note: This list contains packages under planning.
P: Plastic

CE71 (T-Frame)

Package and pin count		0 — 1000 K — 2000 K — 3000 K — 4000 K — 5000 K	Material
LQFP	144	341 K	P
	176	477 K	P
	208	1014 K	P
	256	1358 K	P
HQFP	208	1014 K	P
	240	1188 K	P
	256	1559 K	P
	304	3349 K	P
FBGA	144	341 K	P
	176	477 K	P
	224	1014 K	P
	288	1559 K	P
PBGA	256	1358 K	P
	352	1976 K	P
	420	2794 K	P

Note: This list contains packages under planning.
P: Plastic

CE66 Series

Features

High integration	: Maximum of 1,138,000 BCs
Technology	: 0.35 μm Si-gate, 3- to 4-layer metal wiring
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V +5.0 V ± 10% (only for external interface; when internal requirements is 3.3 V) +3.3 V ± 10% (only for external interface; when internal requirements is 3.3 to 2.0 V)
Gate delay time	: t_{pd} = 98 ps (high-speed type, F/O = 2, standard load)
Gate power consumption	: 0.29 μW/MHz (F/O = 2, standard load)
Junction temperature range	: - 40 to 125°C
High-load driving capability	: I_{OL} = 2 mA/4mA/8mA/12mA/24mA mixable.

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (50 kΩ typical)
Buffer cells dedicated to crystal oscillator
Configurable internal bus circuits
Highly integrated RAM/ROM/multipliers mountable; arbitrary words/bits configurable.
Clock skew layout design method (CDDM) based on the floor plan information minimizes post-layout circuit modification, reducing turnaround time for development.
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supporting development with minimized timing trouble after trial manufacture.
Special interfaces (T-LVTTL and SDRAM-I/F, and others)
Analog PLL
Analog circuits (ADC, DAC, OPAMP and others)
Macros for system ASICs (CPU core, CPU peripheral, operational macros, and others)
Supports DFF scan test with MUX
Supports memory (RAM/ROM) SCAN
Supports memory (RAM) BIST
Supports boundary SCAN

Note: Some items are in preparation.

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.

CE66 (P-frame)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K 1000K 1100K 1200K
TQFP	100	1138K
LQFP	100	1138K
	144	1138K
	176	1138K
	208	939K
QFP	120	1138K
	144	1138K
	160	1138K
	176	1138K
	208	1138K
	240	1138K
	256	1138K
HQFP	208	1138K
	240	1138K
	256	1138K
	304	1138K
PBGA	256	1138K
	352	1138K
FBGA	112	459K
	144	459K
	168	601K
	176	939K
	192	1138K
	224	1138K
	288	1138K

Note: This list contains packages under planning.

CE66 (S-frame)

Package and pin count		0 50K 100K 150K 200K 250K 300K 350K 400K 450K 500K 550K 600K
TQFP	100	112K
LQFP	100	112K
	144	112K
	208	311K
QFP	120	112K
	144	112K
	160	163K
	176	163K
	208	256K
	240	390K
HQFP	208	256K
	240	390K
	256	390K
PBGA	256	390K
	352	579K
FBGA	112	136K
	144	163K
	168	311K
	176	163K
	192	206K
	224	311K
	288	579K

Note: This list contains packages under planning.

CE61 Series

Features

High Integration	: Maximum of 2,000,000 BCs
Technology	: 0. 35 μm Si-gate 3-layer metal wiring/4-layer metal wiring (There are restrictions applicable frames)
Basic circuit (basic cell)	: 2-input NAND/2-input NOR gates
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V High voltage tolerant transistor for I/O; interface provided for 5 V devices (Also requiring a 5 V power supply for interface with 5 V devices)
Gate delay time	: High-speed type, t_{pd} = 85 ps (2-input NAND, F/O = 2, standard load)
Junction temperature range	: 0 to +100°C
High-load driving capability	: I_{OL} = 2 mA/4 mA/8 mA/12 mA/24 mA mixable.
Power consumption	: Reduced to 50% to 20% (over the CE51 Series)

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (Typ. 50kΩ)
Buffer cells for crystal oscillation circuits.
Configurable internal bus circuits
Super high-integration RAM and ROM available. Compilable bit/word configuration
Clock skew reduction layout design technique (CDDM) employed to minimize circuit modification after layout, reducing TAT
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supports development with minimized timing trouble after trial manufacture.
Supports high speed interfaces [P-CML (200 MHz transmission), LVDS (250 MHz transmission), and SDRAM I/F, PCI,5 V tolerant, USB, IEEE 1284]
PLL circuits
Analog circuits (ADC, DAC)
Macros for system ASICs (CPU core and CPU peripheral and operational macros, and others)
Supports tests (for function/DC) using DFF scan with MUX
Supports the test for RAM BIST, RAM SCAN and ROM SCAN
Supports the Boundary SCAN
Now under preparation on for a narrow-pitch pad technology and high-pin count BGA packages to be added to the current lineup
Variety of package options to optimize any gate size

Note: Some items are in preparation.

Number of gates used in each package)

The table below lists the available package types and the reference number of gates used."

CE61 (F10 to F80)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K 1000K 1100K 1200K 1300K	Material
QFP	64	86K	P
	80	86K	P
	100	86K	P
	120	86K	P
	144	593K	P
	160	1317K	P
	160	981K	C
	176	593K	P
	176	1317K	C
	208	1317K	P
	208	1317K	C
	240	981K	P
	240	981K	C
	256	1317K	C
	256	593K	P
	304	1317K	C
LQFP	64	86K	P
	80	86K	P
	100	86K	P
HQFP	208	1317K	P
	240	981K	P
	256	1317K	P
	304	981K	P
BGA	256	593K	P
	352	981K	P
	420	981K	P
PGA	256	1317K	C
	299	1317K	C
	361	981K	C
	401	1317K	C

P : Plastic C : Ceramic

Note: This list contains packages under planning.

CE61 (E7 to E71)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K 1000K 1100K	Material
QFP	120	509K	P
	144	509K	P
	160	747K	P
	176	509K	P
	208	747K	P
	240	747K	P
	256	747K	P
LQFP	64	78K	P
	80	128K	P
	100	128K	P
HQFP	208	1029K	P
	240	1029K	P
	256	1029K	P
	304	1029K	P
BGA	256	391K	P
	352	391K	P
	420	509K	P
	576	747K	P
	672	1029K	P

P : Plastic

Note: This list contains packages under planning.

CG61 Series (Analog PLL embedment is possible in some frames)

Features

High Integration	: 1,560,000 BCs
Technology	: 0. 35 μm Si-gate CMOS, 3-layer metal wiring
Basic circuit (basic cell)	: 2-input NAND/2-input NOR gates
Supply voltage	: +3.3 V ± 0.3 V (normal) to +2.0 V ± 0.1 V (5 V TTL interface is possible when 5 V tolerant I/Os are used.)
Gate delay time	: t_{pd} = 85 ps (3.3 V, 2-input NAND, F/O = 2, standard load)
Gate power dissipation	: 0.24 μW/MHz (2.0 V, 2-input NAND, F/O = 2, standard load)
Junction temperature range	: 0 to +100 °C
High-load driving capability	: I_{OL} = 2 mA/4 mA/8 mA/12 mA/24 mA mixable

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (Typ. 50 kΩ <at 3.3 V>)
Buffer cells for crystal oscillation circuits
Configurable internal bus circuits
Compiled RAM can be embedded. Compilable bit/word configuration
An analog PLL can be embedded in CG61P only.
Clock skew reduction layout design technique (CDDM) employed to minimize circuit modification after layout, reducing TAT
Simulation (before layout) considering the input through rate and detailed RC delay calculation (after layout), supports development with minimized timing trouble after trial manufacture.
Supports high speed interfaces (T-LVTTL, P-CML, LVDS, SDRAM I/F)
Supports tests using DFF scan with MUX
Supports the test for RAM BIST and RAM SCAN

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.

CG 61 (The frame which cannot use Analog PLL)

Package and pin count		0 100K 200K 300K 400K 500K 600K 700K 800K 900K	Material
LQFP	120	222K	P
	144	222K	P
QFP	240	222K	P
	256	395K	P
HQFP	208	802K	P
	240	580K	P
	256	580K	P
	304	802K	P

P: plastic
Note: This list contains packages under planning.

CG 61P (The frame which can use Analog PLL)

Package and pin count		0 20K 40K 60K 80K 100K 120K 140K 160K 180K 200K	Material
LQFP	48	16K	P
	64	88K	P
	80	188K	P
	100	188K	P
	120	188K	P
	144	188K	P
	176	188K	P
	208	188K	P
QFP	240	188K	P
	256	188K	P
BCC	48	88K	P
	64	88K	P

P: plastic
Note: This list contains packages under planning.

CG47 Series

Features

High integration : Maximum 55,000 BCs (on chip)
Technology : 0.65 μm Si-gate CMOS, 2-layer metal wiring
Gate delay time : 300ps (power type 2-input NAND, standard load)
Supply voltage : [Single power supply] +5 V ± 5%(normal), +3.3 V ± 0.3 V (normal)
[Dual power supply] Internal domain: +3.3 V ± 0.3 V, +5 V ± 5% (cannot be mixed)
I/O: +3.3 V ± 0.3 V, +5 V ± 5% (can be mixed)

Interface enabled between dual power sources
Low power consumption enabled by operating internal supply voltage at 3.3V.
Delay time estimation by detailed time equations
Detailed time equations can be used for the estimation of delay time closer to that of actual devices.
Buffer cells for crystal oscillations circuits
Supports separate low frequency (32 kHz), and high frequency (1 to 40MHz) buffers, and oscillator stop function.
Supports output open drain cell and input fail safe cells
Compiled cells include single port RAM, dual port RAM, and FIFO memory.
Note: The type of the RAM that can be used is specified depending on the internal power supply when the RAM is a single-port RAM.
HISCAN (scan circuit automatic generation function)
HISCAN is supported with single power supply, but dual power supply specifications and HISCAN are mutually exclusive.
Simple interface
CAD-to-CAD interface uses special language for logic data (FLDL) and test data (FTDL).
Integrated development tools

Number of gates used in each package

The table below lists the available package types and the reference number of gates used.

Package and pin count		0 5K 10K 15K 20K 25K 30K 35K 40K 45K 50K
SSOP	30	2K
LQFP	48	11K
	64	21K
	80	33K
	100	33K
	120	33K
	144	33K
	176	33K
	208	33K
QFP	64	21K
	80	21K
	100	21K
	240	33K
BCC	48	21K
	64	31K
	80	31K

Note: This list contains packages under planning.

ASIC

CG46 Series

Features

High integration	: Maximum 198,084 BCs (on chip)
Technology	: 0.65 μm Si-gate CMOS, 2-layer metal wiring
Basic circuit (basic cell)	: 2-input NAND/2-input NOR gates
Input level	: TTL/CMOS level mixable
Supply voltage	: +5 V ± 5% (normal) +3.3 V ± 0.3 V (optional)
Gate delay time	: Standard gate tpd = 360 ps (2-input NAND, standard load) Power gate tpd = 300 ps (2-input NAND, standard load)
Operating temperature	: 0 to +70°C
High-load driving capability	: I_{OL} = 3.2 mA/8 mA/12 mA/24 mA mixable

Output buffer cells with noise reduction circuits
On-chip input pull-up/pull-down resistors (Typ. 50 kΩ)
Buffer cells for crystal oscillations circuits
Configurable internal bus circuits
RAM and FIFO memory allowing arbitrary bit/word configuration
Clock skew reduction layout design technique (CDDM) employed to minimize circuit modification after layout, reducing the period of time for development
Delailed RC delay calculation minimized timing trouble after trial manufacture.
Supports ATG (Automatic Test Generation) based on scan design
Supports HISCAN (automatic scan generation)
Simplified interface: CAD-to-CAD interface uses special language for logic data (FLDL) and test data (FTDL) .
Integrated development tools

Number of gates used in each package

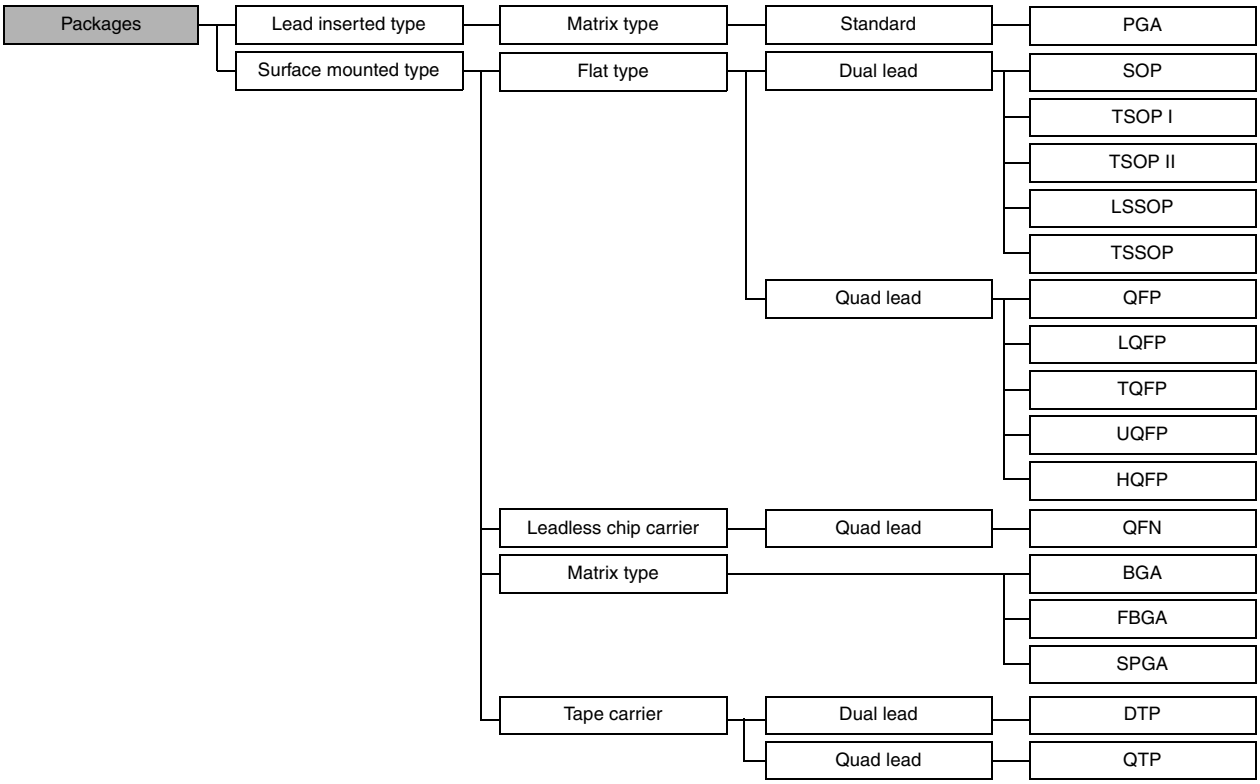
The table below lists the available package types and the reference number of gates used.

Package and pin count		Number of gates used (BC)
		0 10K 20K 30K 40K 50K 60K 70K 80K 90K 100K
SSOP	30	5K
LQFP	48	10K
	64	42K
	80	42K
	100	50K
	120	65K
	144	50K
	176	50K
	208	50K
QFP	44	5K
	64	65K
	80	65K
	100	65K
	208	89K
	240	89K

Note: This list contains packages under planning.

■ Package Line-up

The packages are classified as follows, according to form, material, and the mounting methods for which they are suited.



Package Line-up

Name of package	Description	Lead pitch (mm)
PGA	Pin Grid Array Package	1.27/2.54
SOP	Small Outline Package (straight lead) Small Outline L-Leaded Package	1.27
SOL*2	Small Outline L-Leaded Package (JEDEC*1)	1.27
SSOP	Shrink Small Outline L-Leaded Package	0.65/0.80/1.00
TSOP (I)	Thin Small Outline L-Leaded Package (I)	0.50/0.55/0.60
TSOP (II)	Thin Small Outline L-Leaded Package (II)	0.50/0.80/1.00/1.27
SON	Small Outline Non-Leaded Package	0.50/1.00
QFP	Quad Flat Package (straight lead) Quad Flat L-Leaded Package	0.40/0.50/0.65/0.80/1.00
LQFP*2	Low-Profile Quad Flat L-Leaded Package	0.40/0.50/0.65/0.80
TQFP	Thin Quad Flat L-Leaded Package	0.40/0.50
HQFP	QFP with Heat Sink	0.40/0.50/0.65
LCC*2	Leadless Chip Carrier	1.016/1.27
QFN	Quad Flat Non-Leaded Package	
BGA	Ball Grid Array	1.27/1.0
FBGA	Fine pitch Ball Grid Array	0.8/0.75/0.65/0.5
DTP	Dual Tape Carrier Package	—
QTP	Quad Tape Carrier Package	—

*1: Joint Electron Device Engineering Council

*2: Package name used by Fujitsu Microelectronics

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○ S30MS512R25TFW00	70	-
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T021 series	12	-
V08 series	12	-
V09 series	12	-
V10x series	12	-
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